



A10-USB_BOARD_ V01

1. Schematic Index
2. SYSTEM BLOCK
3. Placement
4. USB+SPK+MIC+VIB+TPCHR+ANT
5. PIR of EE

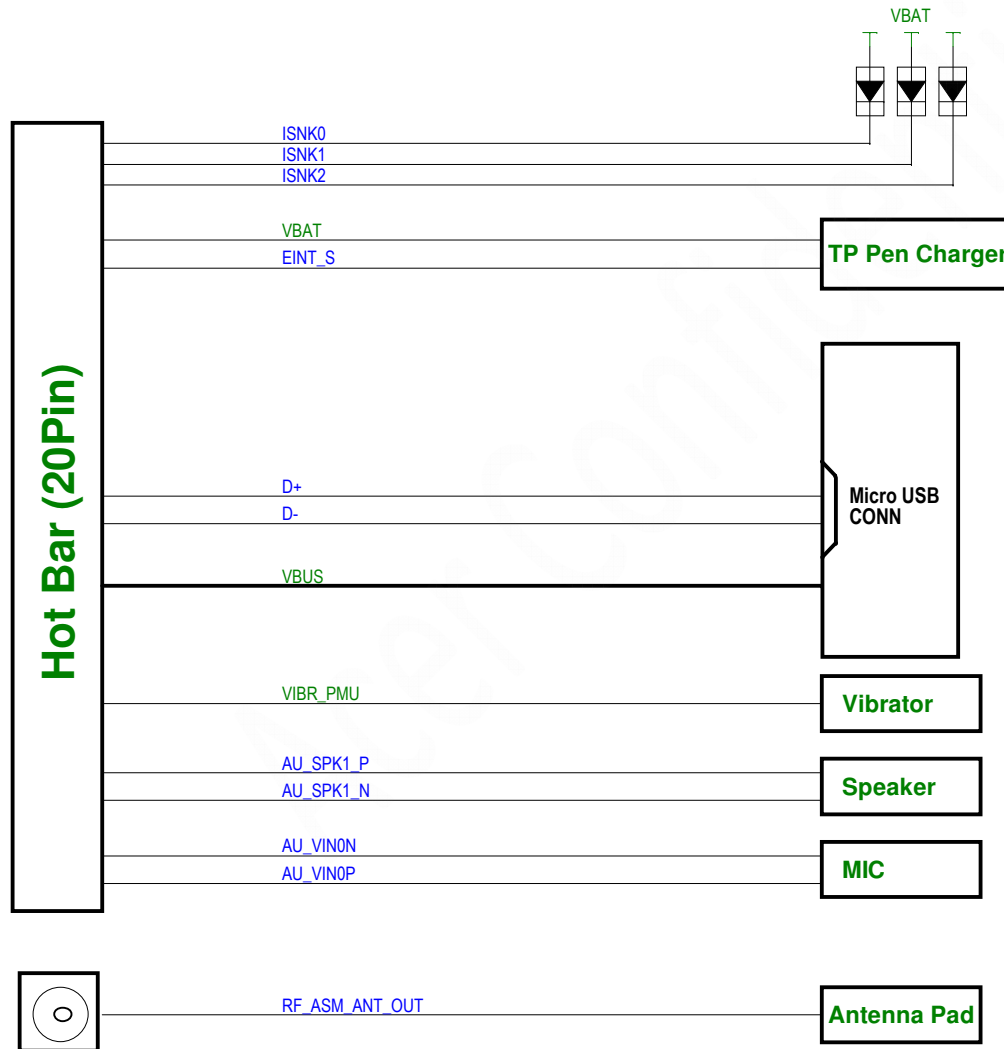
VERSION HISTORY

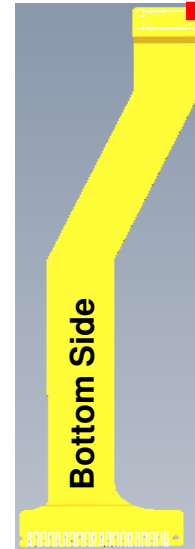
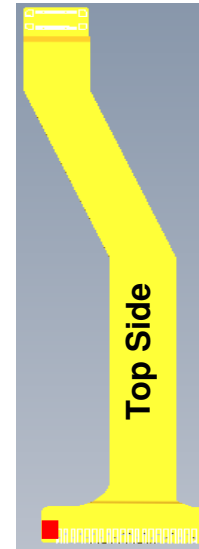
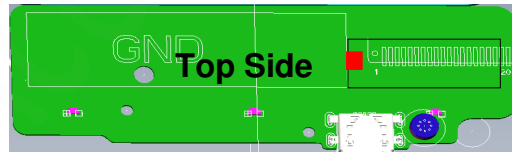
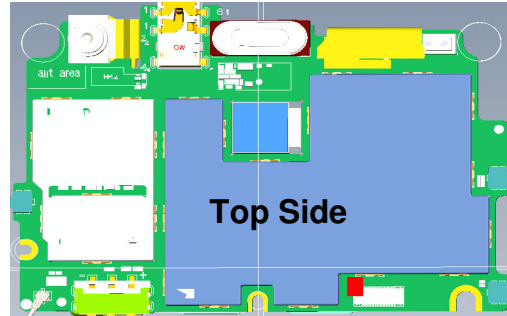
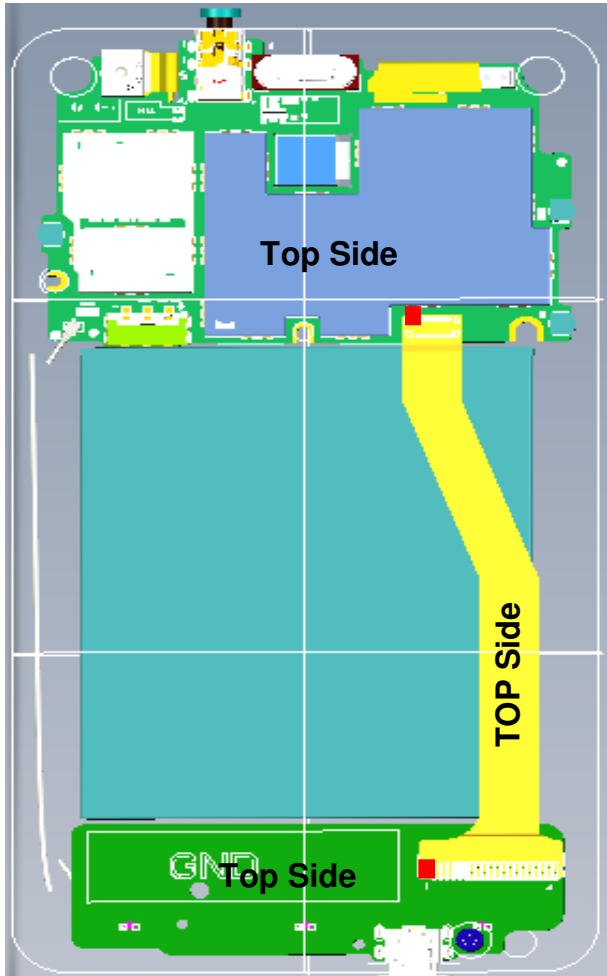
Version	DESIGN PHASE	DESCRIPTION

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	Title: SCHEMATIC INDEX		Allegro Lib Ver
	Size: C	Document Number: A10 USB BOARD	OrCAD Lib Ver
	Approved:  Designer: Hill	Date: Friday, May 10, 2013	Rev V0.1

Sheet 1 of 5

System Block



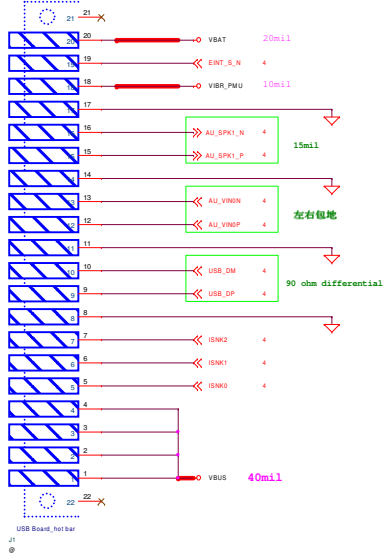


PCB LAYER

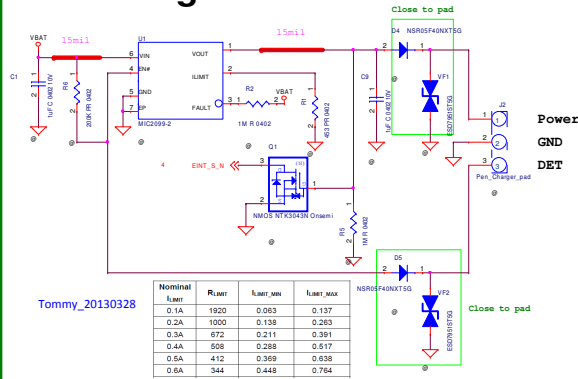
TOP
GND1
GND2
BOTTOM

acer		Acer Inc.		Drawing Rule
Project:	A10	File:	Placement	Align Lib Ver
Doc ID	Document Number:	A10 USB BOARD	Rev	V0.1
Designer	MS	Date	Friday, May 16, 2014	Sheet 9 of 9

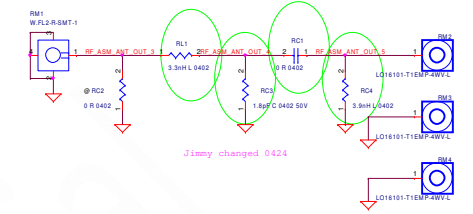
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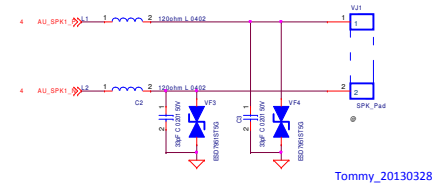
PEN Charger



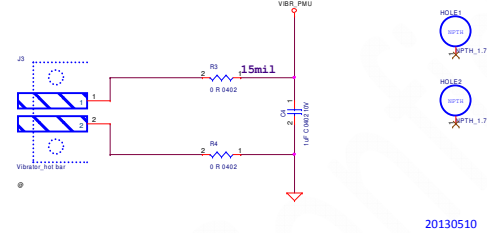
Antenna



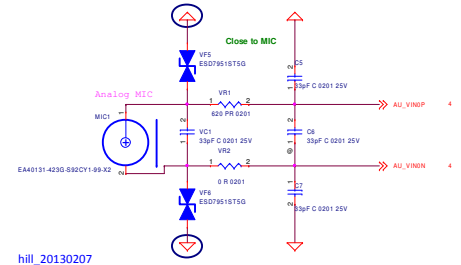
Speaker



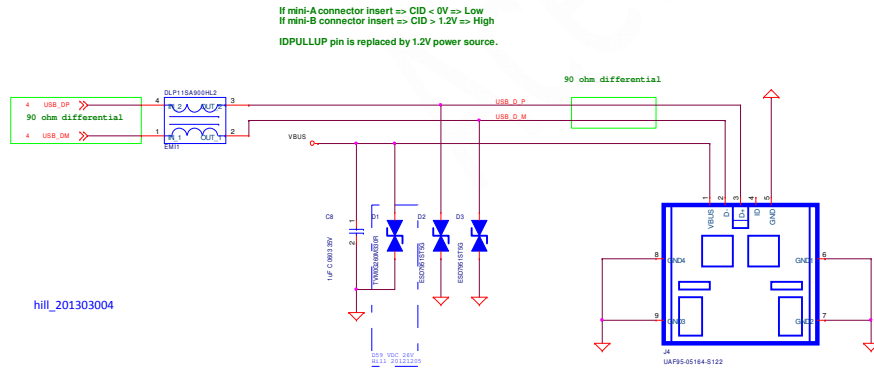
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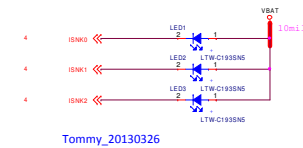
MIC



USB Connector




TP LED



PIR of EE

SCHEMATIC-REV	PCB-REV	DATE	SHEET	CONTENTS	REMARK



Acer Inc.

Project: A10

Title: PIR of EE

Document Number: A10 USB BOARD

Rev: V0.1

Reviewed: _____

Design: H8

Drawn: _____

Date: Friday, May 15, 2015

Checked: _____

Sheet: 5 of 5

Drawing Rule: Align to Vis

DWG to Vis