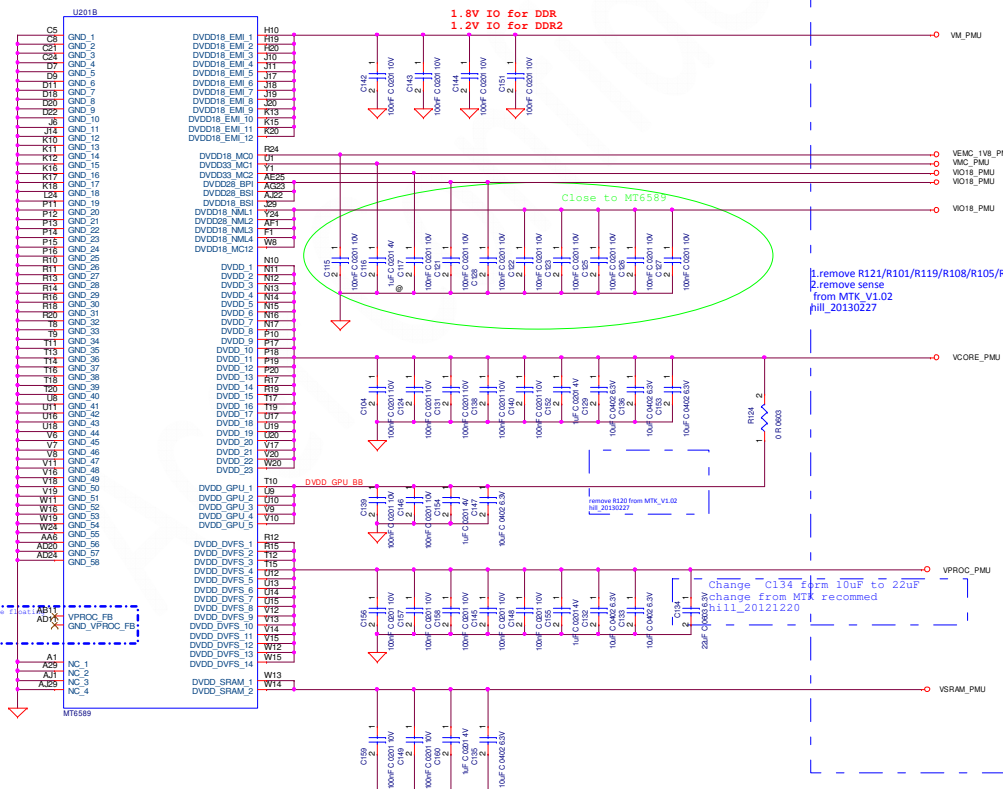
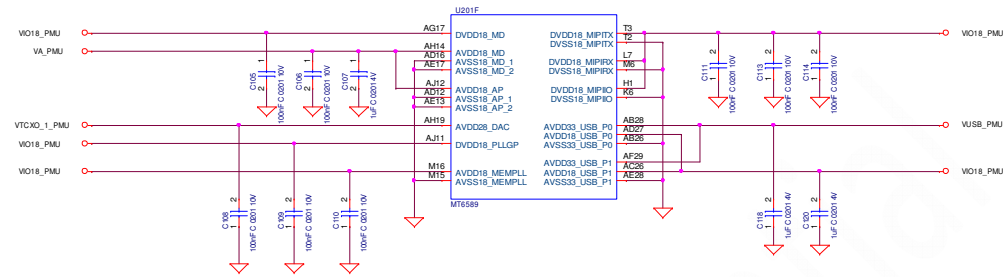


Remove R110~R111/R113~R118  
chng from MTK\_V1.0 recoment  
hill\_20130103

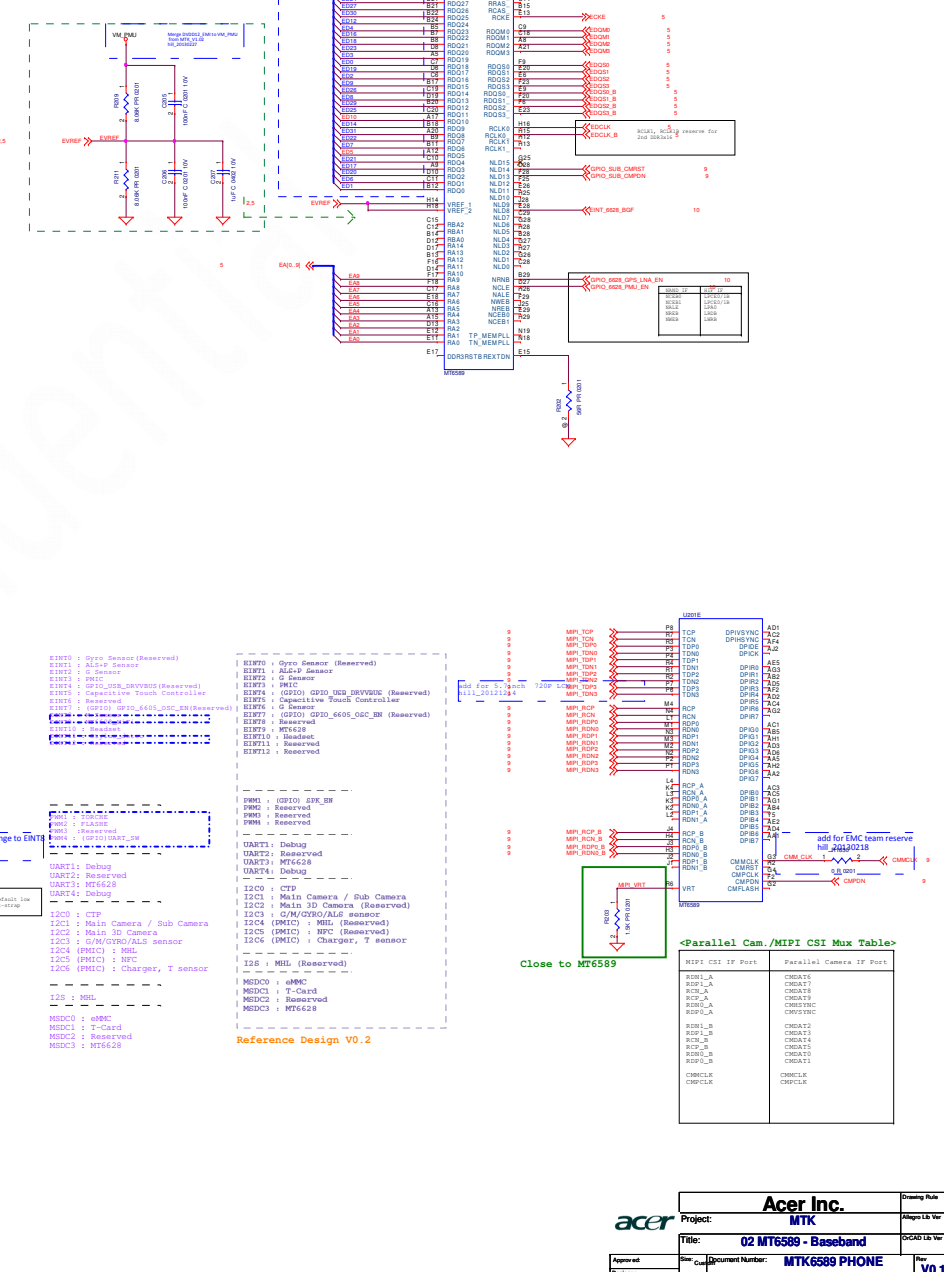
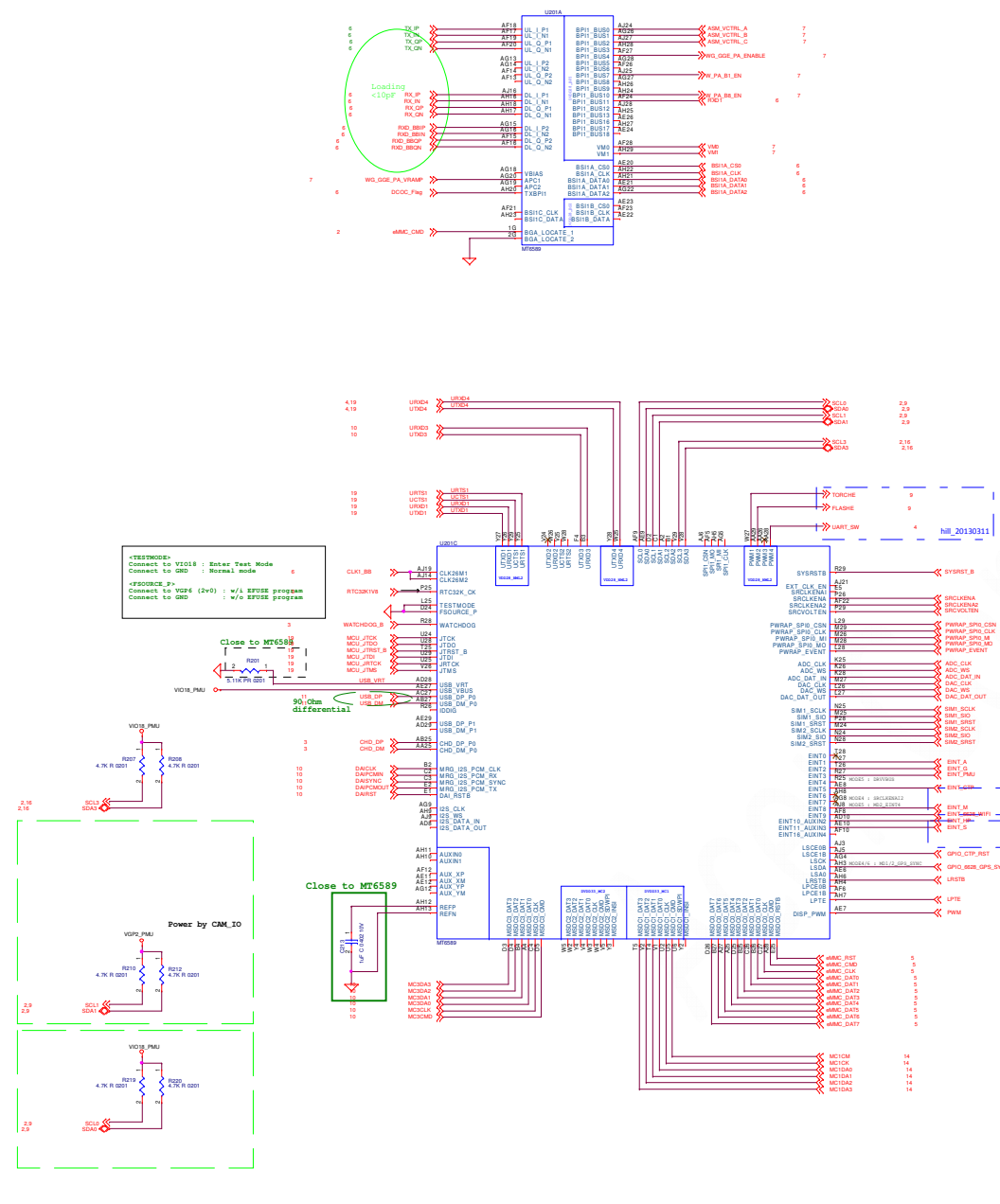


Modify MT6589 VPROC\_FB (pin AB11) & GND\_VPROC\_FB (pin AD11) to be floating  
change from MTK\_V0.21  
Hill 20121205

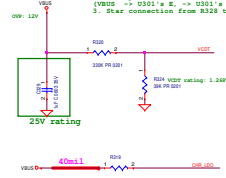
1.remove R121/R101/R119/R108/R105/R106/R109/R102  
2.remove sense  
from MTK\_V1.02  
hill\_20130227

```
remove R120 from MTK_V1.02
bill_20130227
```

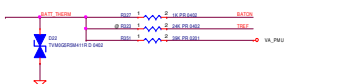
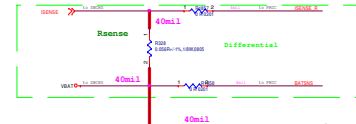
Change C134 from 10uF to 22uF  
change from MTK recomm



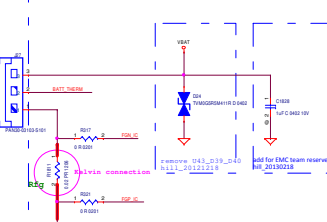
1. Close to Battery Connector.  
(Rsense (R328) <10mm)
2. Main path should be 40mil.  
(VBUS -> U301's E, -> U301's C -> R328 -> VBAT)
3. Star connection from R328 to BAT Connector



Switching charger : R328 use 56n ohm  
Pulse charger : R328 use 0.2 ohm



## hill 20130218



**Close to Switching charger**

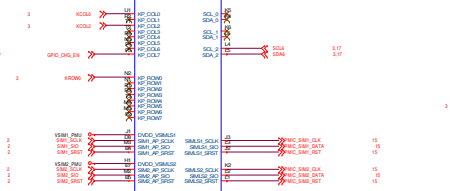
VOLT\_PMR

R205 4.7K R 0201

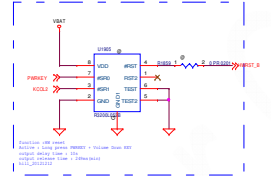
R206 4.7K R 0201

SCL6 SDA6

## Digital

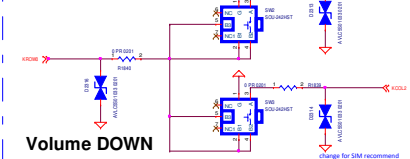


## Power Key



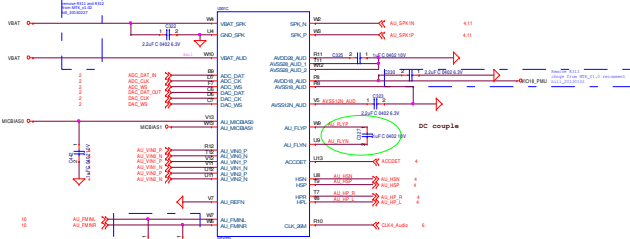
DO NOT put pull-up resistor on PWRKEY

**Volume UP**



**Volume DOWN**

## Audio

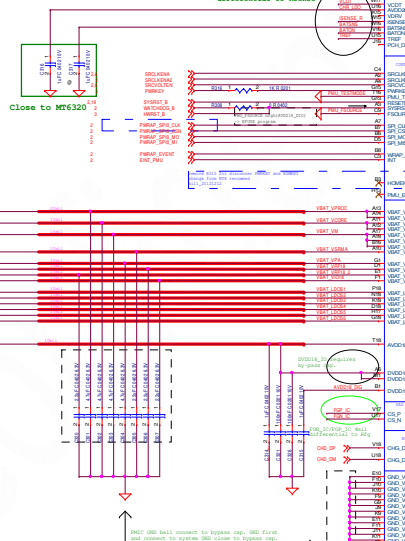


**Volume KEY**



Symbol	LPDDR2/1.2V	DDR3U/1.25V	DDR3L/1.35V	DDR3/1.5V
VM_SEL1	L	H	L	H
VM_SEL2	L	L	H	H

ISENSE/BSTENS 4mil  
differential to Bsense

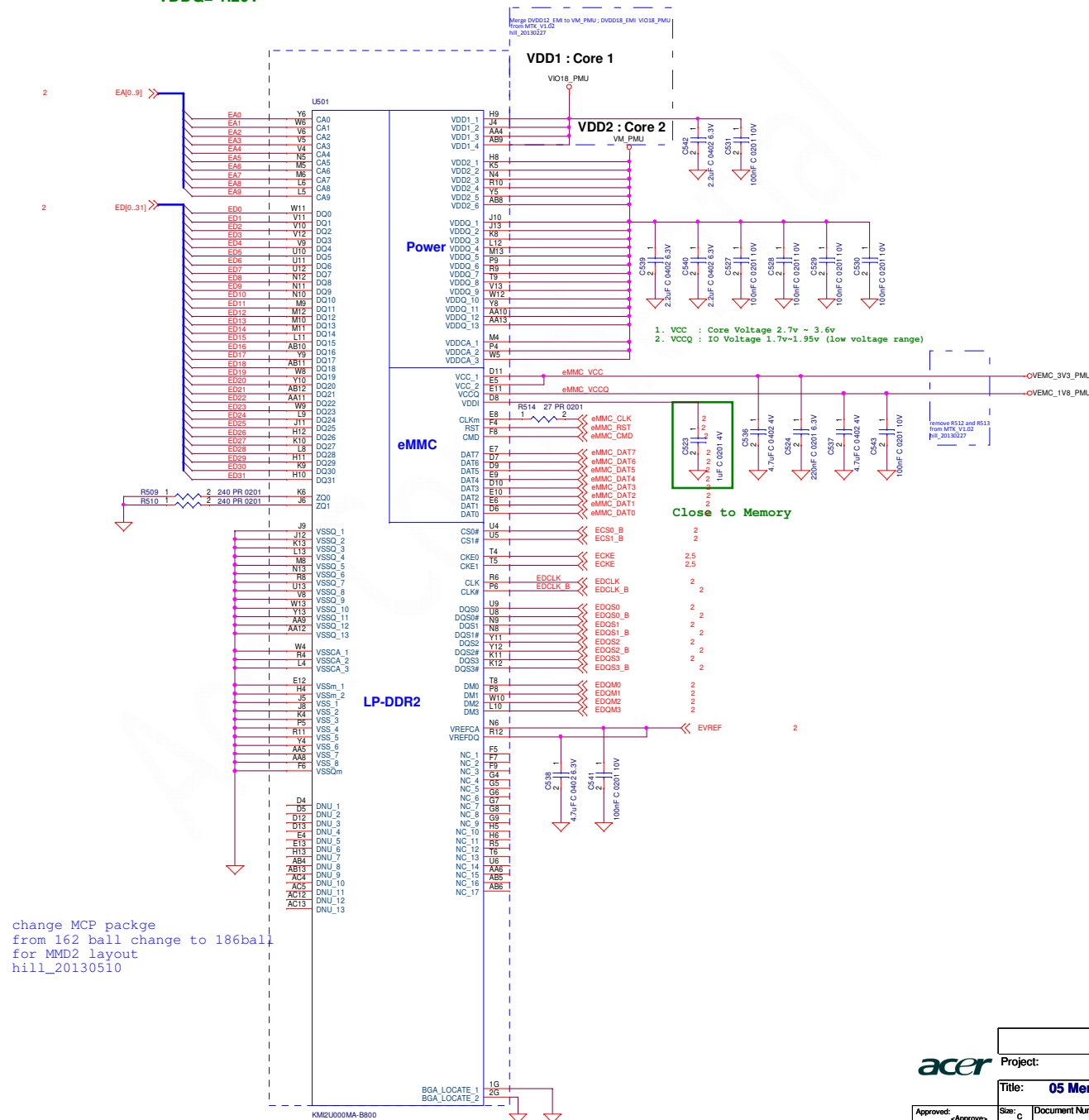


↑  
PGC GND ball connect to bypass cap. GND first  
and connect to system GND close to bypass cap.

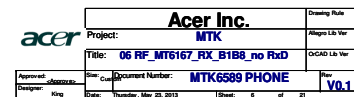
	Symbol	Application	Value (V)	Current (mA)	Cap. Value (uF)
Buck	VPW01	CPU	0.7-1.25 (DC/DC)	2000	42
	VCC010	Memory/Infra	0.7-1.25 (DC/DC)	1200	30
	VM	VM	1.2/1.28/1.35/1.5	1100	10
	VDRAM	Memory	0.7-1.25 (DC/DC)	600	10
	VPA	320A	0.5-1.4 (100W/step)	5	2-2x2.2
	VPF18	1st BP	1.825	450	4.7
	VPF18	2nd BP	1.825	450	4.7
	VPF18	3rd BP	0.7-1.25 (50W/step)	47	10x10
	VP1018	10 App.	1.8	600	4.7
	VM		0.7-1.25/5	1500	
Analog LDO	VPF28-1	HD575	2.85	300	2.2
	VPF28-2	General	1.8/2.85	300	2.2
	VPF30-1	HD575	3	40	1
	VPF30-2	HD575	1.8/2.8	40	1
	VCC010	VCMA	1.5/1.8/2.5/2.8	200	2.2
	VCC010	VCMA	3	200	2.2
Digital LDO	VPF46	MT6168	0.9/1.0/1.1/1.2	300	2.2
	VAMP		3	200	1
	VDCS		1.8/3	200	1
	VDCS	T-Card	3	200	1
	VDCS	T-Card	3	200	1
	VDCS	4inMC (Cores)	3.0/3.3	800	4.7
	VDCS_V18		1.2/1.3/1.5/1.8/2.5/2.8/3.0/3.3	200	2.2
	VDCS_V18		1.2/1.3/1.5/1.8/2.5/2.8/3.0/3.3	400	2.2
	VPF2	VCMA-10	1.2/1.3/1.5/1.8/2.5/2.8/3.0/3.3	200	2.2
	VPF05	VCMA_XF	1.2/1.3/1.5/1.8/2.5/2.8/3.0/3.3	200	1
	VPF5	CPY/CHM0	1.2/1.3/1.5/1.8/2.5/2.8/3.0/3.3	200	1
	VPF5	CPY/CHM0	1.2/1.3/1.5/1.8/2.5/2.8/3.0/3.3	200	1
Vibrator	VPF18	VSIM1	1.2/1.3/1.5/1.8/2.5/2.8/3.0/3.3	200	1
	VPF18	VSIM2	1.2/1.3/1.5/1.8/2.5/2.8/3.0/3.3	200	1
	VPF18	VSIM3	1.2/1.3/1.5/1.8/2.5/2.8/3.0/3.3	200	1
	VPF18	VSIM4	1.2/1.3/1.5/1.8/2.5/2.8/3.0/3.3	200	1



VDD1=1.8V  
VDD2=1.20V  
VDDCA=1.2V  
VDDQ= 1.20V




```
change MCP packge |
from 162 ball change to 186ball |
for MMD2 layout |
hill_20130510 |
```





1

	<b>Acer Inc.</b>		Drawing Rule	
	Project: <b>MTK</b>		Allegro Lib Ver	
Title: <b>07 RF_TX_ASM_B1B8</b>		Grd Lib Ver		<b>V0.1</b>
Approved: <i>-aappp-</i>	Date:	Document Number: <b>MTK6589 PHONE</b>		
Designer: <i>Kina</i>	Date: <b>Thursday, Mar 23, 2011</b>	Sheet: <b>7</b>	of: <b>21</b>	

Acer Confidential



Project:		Acer Inc.		Drawing Rule
Title:		MTK		Allegro Lib Ver
Document Number:		08 Reserved		OrCAD Lib Ver
Approved: <Assumes>	Slas: Custom	Document Number: MTK6589 PHONE		Rev
Designer: King	Date: Thursday, May 23, 2013	Sheet: 8	of 21	V0.1



## CTP



### Sub Camera



Main Camera / Sub Camera share power domain design should double check the voltage level is compatible

## Backlight LED Drive

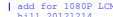
## Main LCM



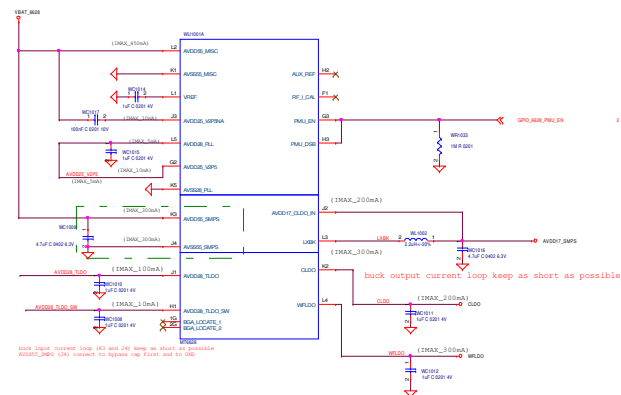
## Flash LED



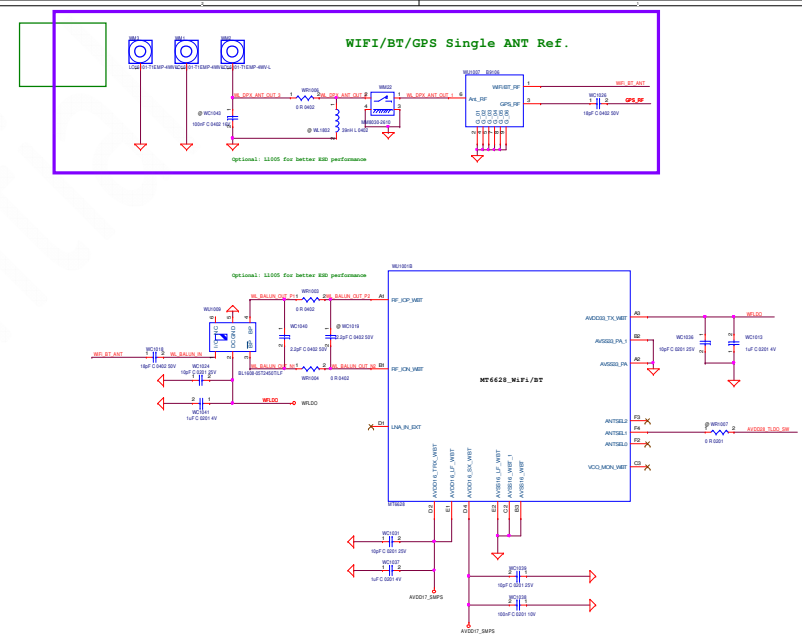
## Main Camera



## MT6628\_PMU



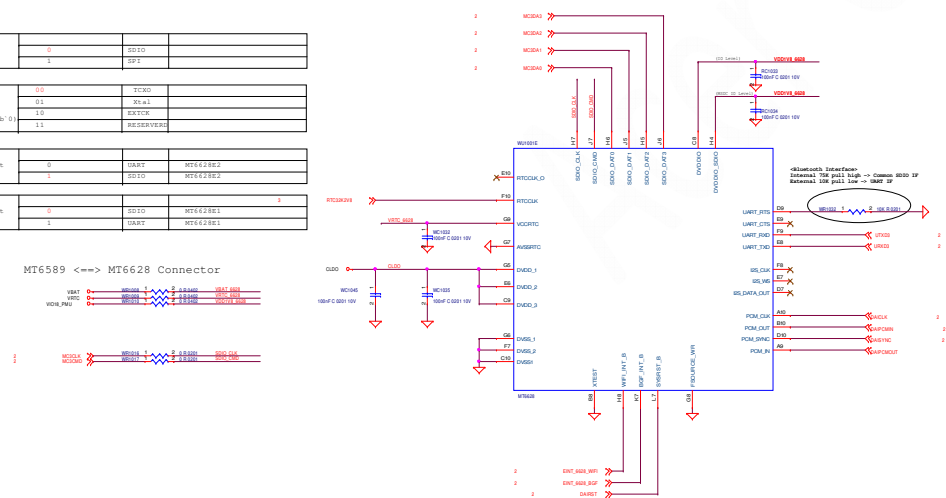
## MT6628\_BT/WiFi



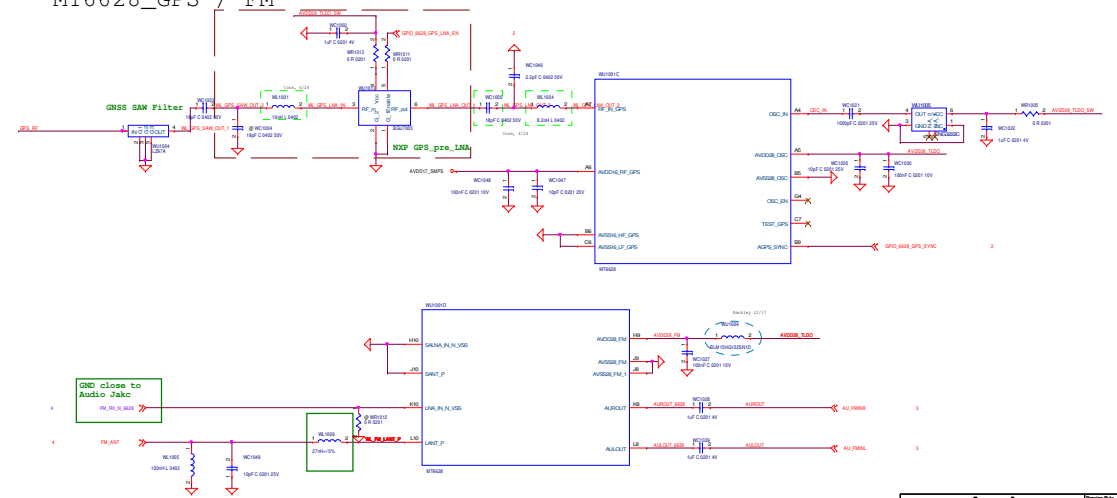
## MT6628\_GPIO

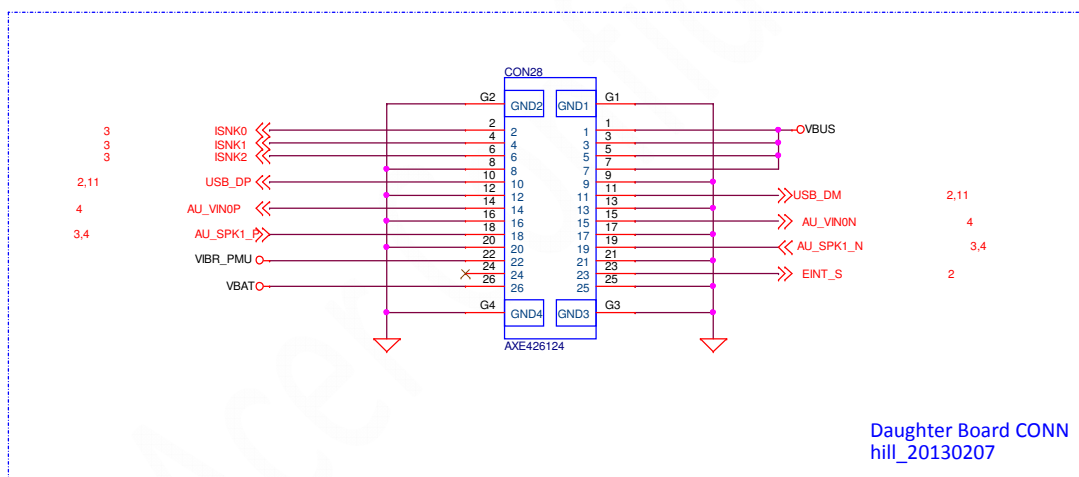
WIFF_What			
ANTSEL-0	0	0000	
	1	0011	
Xtal1/OSC	00	0000	
ANTSEL-1 (N 0)	01	0011	
	10	0100	
	11	01010100	
RT/CON Busy	0	0001	00000000
UART_RTS	0	0000	00000000
RT/CON Status	0	0000	00000001
ANTSEL-0	1	0001	00000001

MT6589 <==> MT6628 Connector

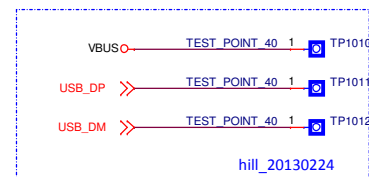


## MT6628\_GPS / FM






remove OVP  
hill\_20130218



acer

Acer Inc.		Drawing Rule	
Project:	MTK	Allegro Lib Ver	
Title:	11.USB	OrCAD Lib Ver	
Approved: <Approve>	Size: Custom	Document Number: MTK6589 PHONE	Rev V0.1
Designer: King	Date: Thursday, May 23, 2013	Sheet: 11	of 21



	Project: <b>Acer Inc.</b>		Drawing Rule
	Project: <b>MTK</b>		Allegro Lib Ver
	Title: <b>12. NFC_MT6605 (Reserved)</b>		OrCAD Lib Ver
	Size: C Document Number: <b>MTK6589 PHONE</b>		Rev <b>V0.1</b>
Approved: <b>&lt;Approve&gt;</b>	Designer: King	Date: Thursday, May 23, 2013	Sheet: 12 of 21

5

4

3

2

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D

C

B

A

5

4

3

2

1

Project: MTK

Title: 13 Reserved

Approved: <Approve>

Designer: King

Size: Custom

Date: Thursday, May 23, 2013

Document Number: MTK6589 PHONE

Sheet: 13 of 21

Drawing Rule

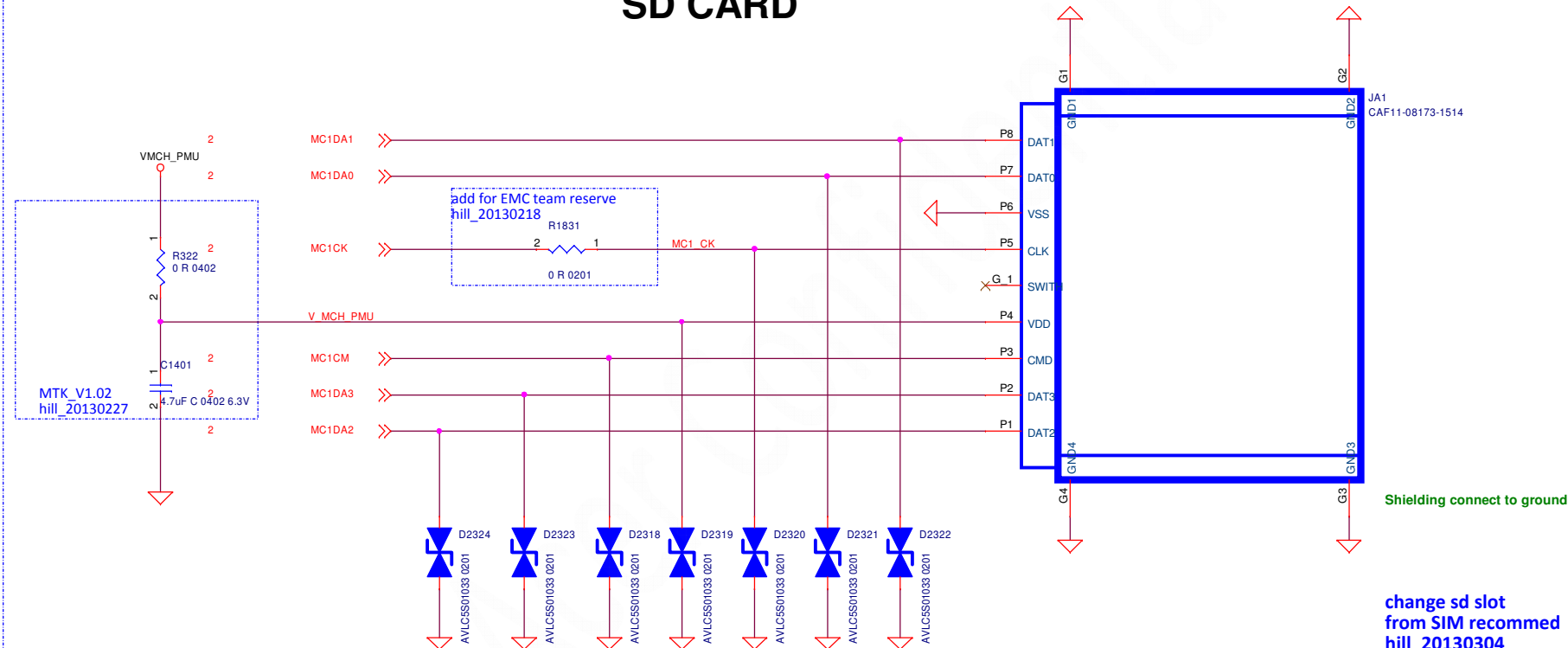
Allegro Lib Ver

OrCAD Lib Ver

Rev V0.1

Acer Confidential

# SD CARD



acer

Acer Inc.

Project:	MTK	Drawing Rule
Title:	14 Memory CARD	Allegro Lib Ver
Size:	Custom	OrCAD Lib Ver
Document Number:	MTK6589 PHONE	Rev
Date:	Thursday, May 23, 2013	Sheet: 14 of 21

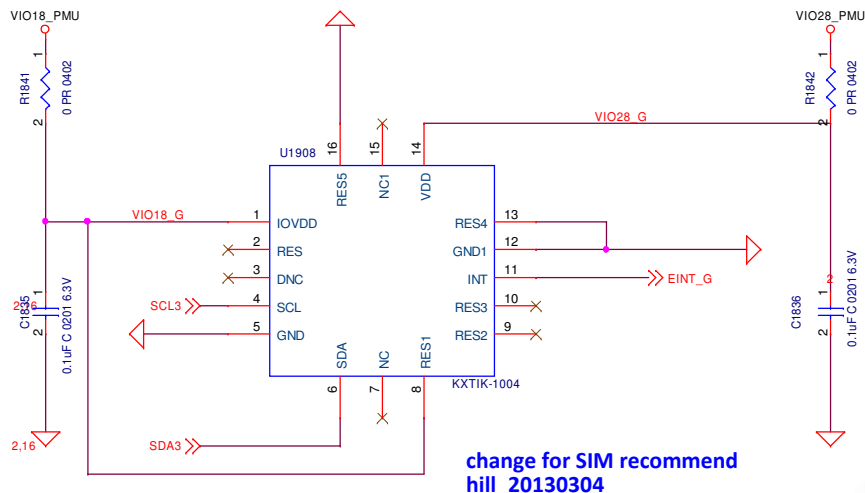
Approved:	<Approve>
Designer:	King

V0.1



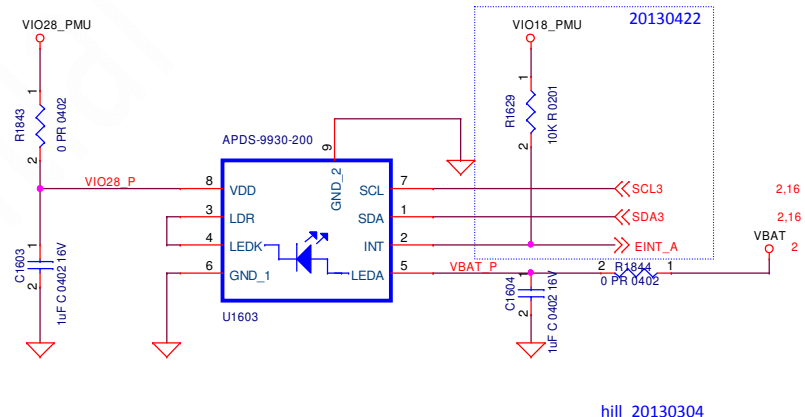
## G-Sensor

The Slave Address associated with the KXTIK is 0001111.



## ALS & PS Sensor

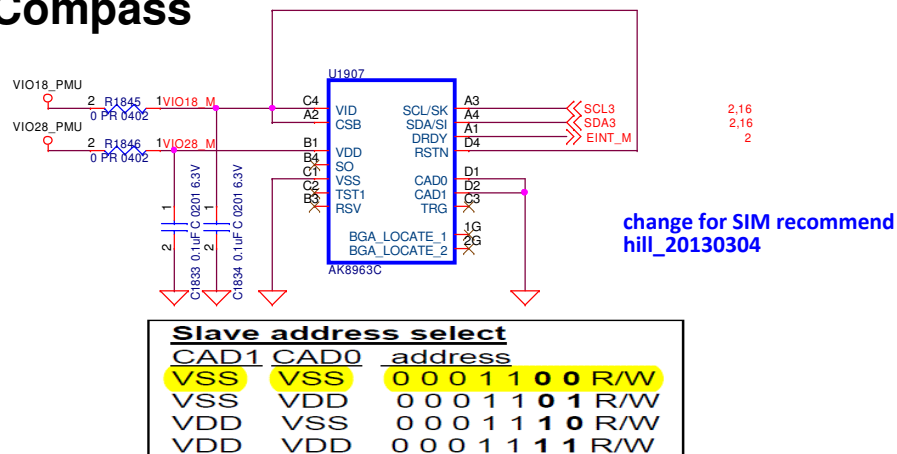
I2C Address: 0x39 (Write:0x72, Read:0x73)



## Gyro Sensor

I2C Address: 0x68 (Write:0xD0, Read:0xD1)

## e-Compass



Slave address select		
CAD1	CAD0	address
VSS	VSS	0 0 0 1 1 0 0 R/W
VSS	VDD	0 0 0 1 1 0 1 R/W
VDD	VSS	0 0 0 1 1 1 0 R/W
VDD	VDD	0 0 0 1 1 1 1 R/W

acer

Acer Inc.

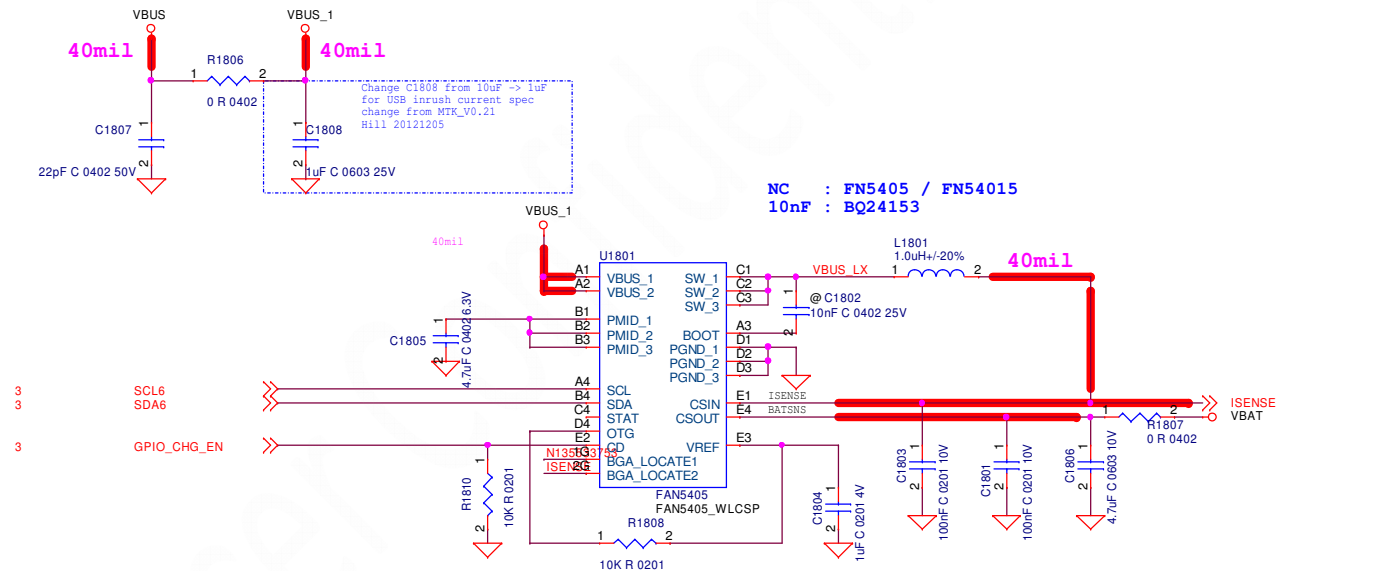
Project:	MTK	Drawing Rule
Title:	16 Sensors, OFN (Key)	Allegro Lib Ver
Size:	Custom	OrCAD Lib Ver
Document Number:	MTK6589 PHONE	Rev
Date:	Thursday, May 23, 2013	Sheet: 16 of 21

Approved: <Approve>  
Designer: King

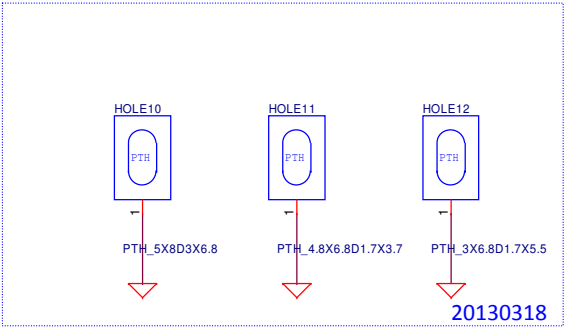
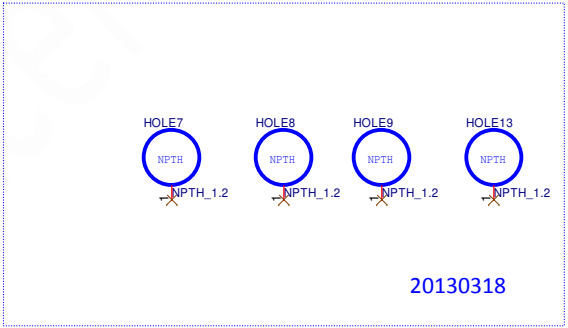
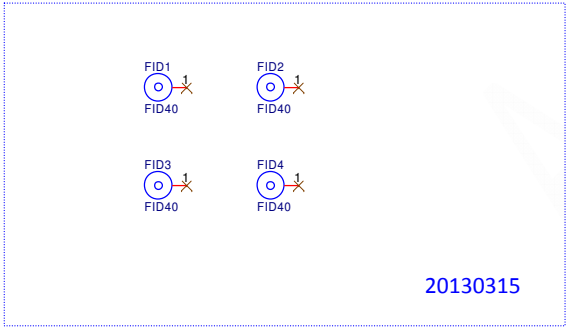
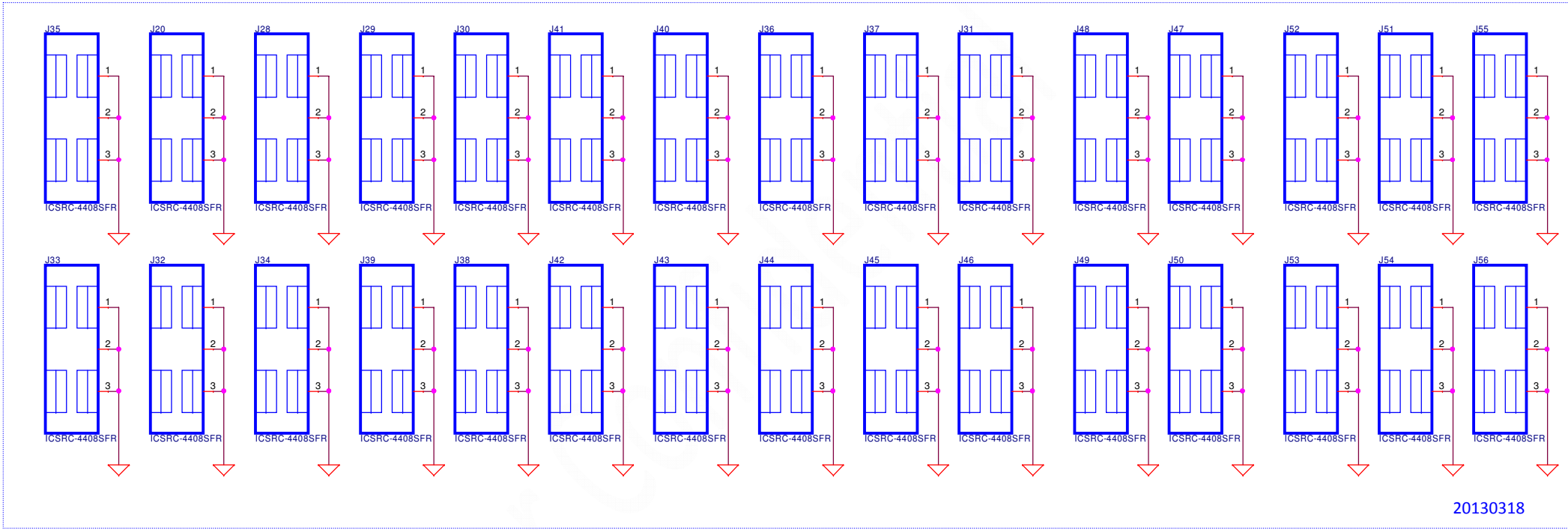
V0.1



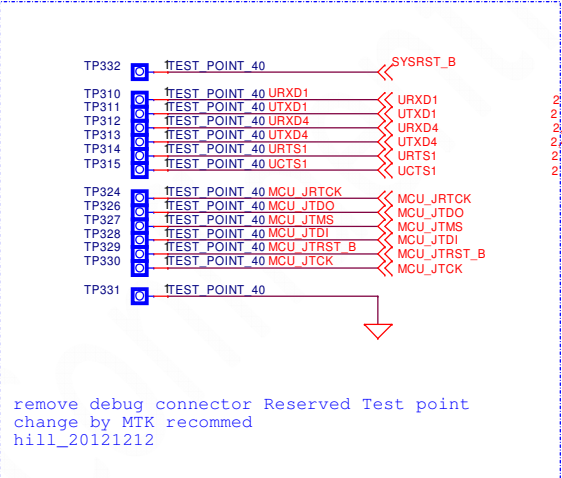
## Switching Charger



If switching charger is used:  
(1) R1801~R1805, C1801~C1806, L1801, U1801 are needed  
(2) U303, U304 change to NC

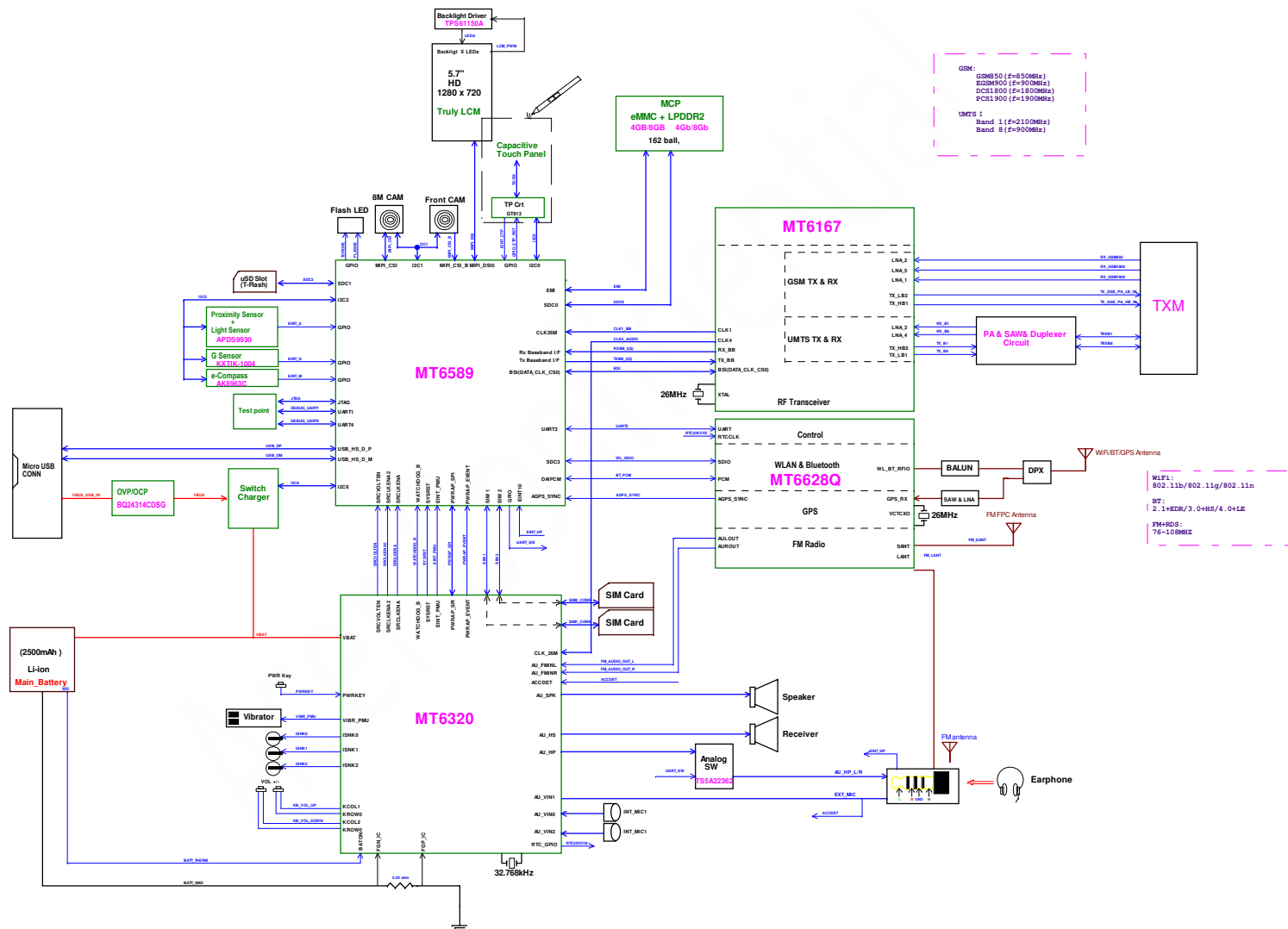


Acer Inc.		Drawing Rule
Project:	MTK	Allegro Lib Ver
Title:	19 Reserved	OrCAD Lib Ver
Approved:	Size: Custom	Document Number: MTK6589 PHONE
Designer: King	Date: Thursday, May 23, 2013	Rev V0.1
Sheet: 18 of 21		



Acer Inc.		Drawing Rule	
Project:	MTK	Allegro Lib Ver	
Title:	20 Debug	OrCAD Lib Ver	
Approved: <Approve>	Size: Custom	Document Number: MTK6589 PHONE	Rev V0.1
Designer: King	Date: Thursday, May 23, 2013	Sheet: 19	of 21

## A10 System Block Diagram



Reference	Version	Category	Item
A10 MB V02		page 03	add C1837 and C1838
A10 MB V02		page 16	change R1629 pin2 connect to U1603 pin 2
A10 MB V02		page 03	add C1839 and C1840 / change TR1 PAD size
A10 MB V02		page 03 , 04	change Net AU_HP_R and AU_HP_L connect to VU2 pinC1 and pin C3 Vu2 .pin B1 and pin B3 connect to Vp3002 pin B1 and pin A1 VP3002 pin B3 and pin A3 connect to phone net AU_HPR_F and AU_HPL_F
A10 MB V02		page 04	delete TP309 and VR2921 and VR2917 and VC2918
A10 MB V02		page 04	change VL3005 and VL2906 and VL3005 to BLM15HD1825N1_0402
A10 MB V03		page 05	change U501 emmc_LPDDR2 MCP from 162 ball chanege to 186 ball
A10 MB V1.0		page 04	add R1860 and R1861