Sheet #	Content
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2	Revision History
3	Block Diagram
4	GPIO Map
5	MSM8x12_Control_1
6	MSM8x12_Control_2
7	MSM8x12_GPIO
8	MSM8x12_Power_1
9	MSM8x12_GND
10	PM8110_PWR
11	PM8110_Control
12	WTR2605_Primary path
13	WTR2605_Power_Primary path
14	WTR2605_TXM_Primary path
15	UMTS B1_Primary path
16	UMTS B8_Primary path
17	PRX Matching_Primary path

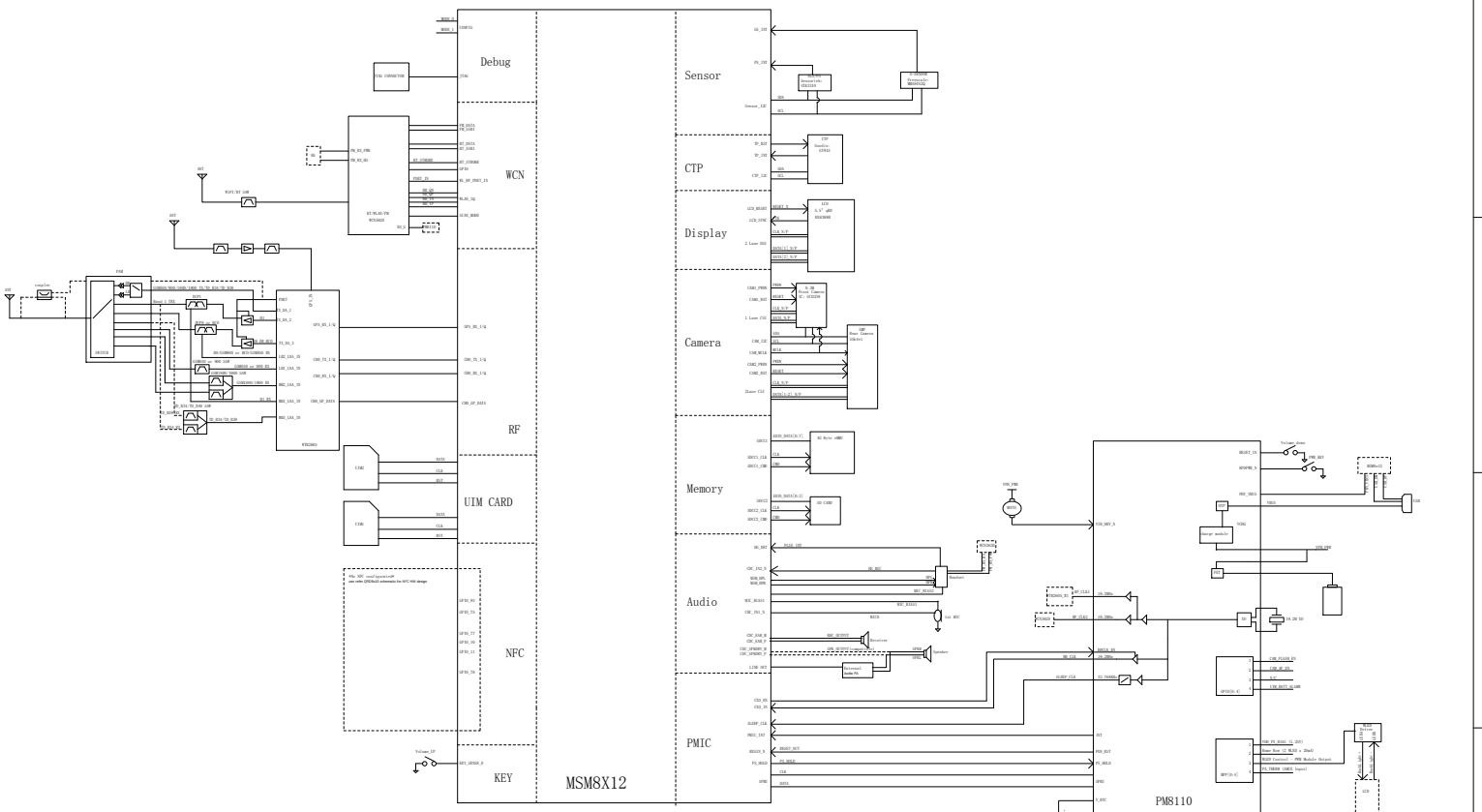
Sheet #	Content
18	WIFI/BT
19	GPS/APT/XO distribution
20	NFC
21	Audio
22	Sensors
23	Memory
24	MultiMedia
25	Interface
26	Change List1
27	Change List2

TITLE:	88100_1_12(Z100)	REV:	DVT
DOCUMENT NO.:	GJ_TABLE_OF_CONTENTS	SIZE:	A3
DEPARTMENT:	Hardware DEPT.		
COMPANY:	WINGTECH		
DESIGNER:	Last Saved Date: 2015/5/5	SHEET	1 OF 27

Revision History

HW Vevision	Doc Revision	Date	Description of Change
EVT	A	May. 2013	Initial release
DVT1	B	Aug. 2013	DVT1 initial release, please refer to Item 1 to Item 96 in "Change List1 " page
DVT2	C	Sep. 2013	DVT2 initial release, please refer to Item 1 to Item 108 in "Change List2 " page
DVT2	D	Jan. 2014	DVT2 updated release, please refer to Item 109 to Item 125 in " Change List 2" page

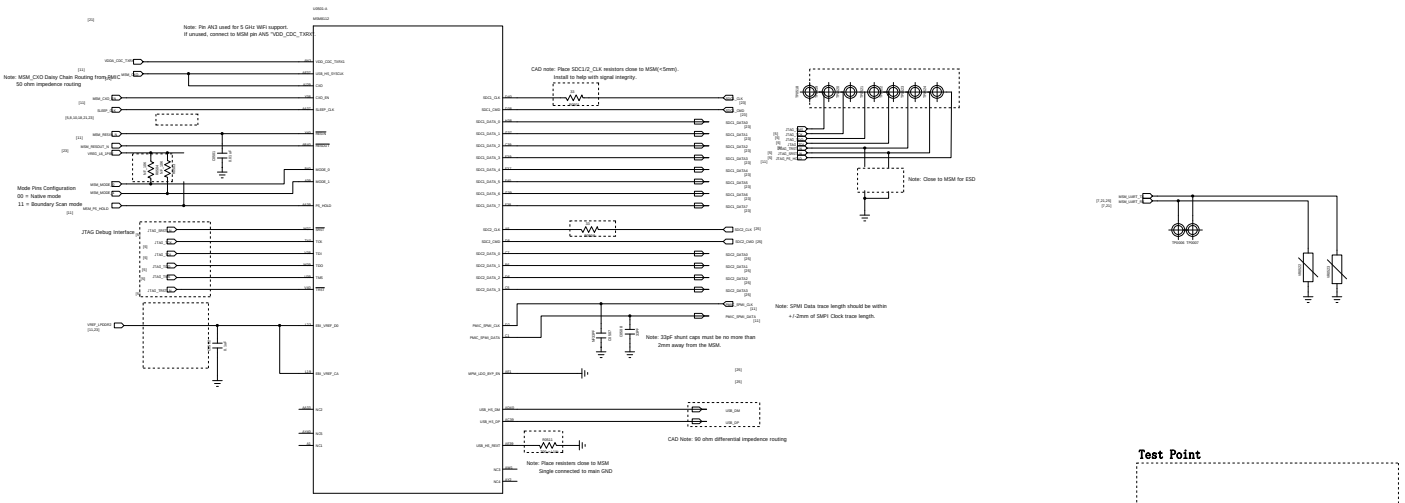
TITLE:	88100_1_12(Z100)	REV:	DVT
DOCUMENT NO.:	02_REVISION_HISTORY	SIZE:	A3
DEPARTMENT:	Hardware DEPT.		
COMPANY:	WINSTECH		
DESIGNER:	Last Saved Date: 2013/5/9	SHEET	2 OF 27



TITLE:	88100_1_12(2300)	REV: OVT
DOCUMENT NO:	03_BLOCK_DIAGRAM	SIZED: A3
DEPARTMENT:	Hardware DEPT.	
COMPANY:	WINGTECH	
DESIGNER:	Last Saved Date: 2015/5/6	SHEET 3 OF 27

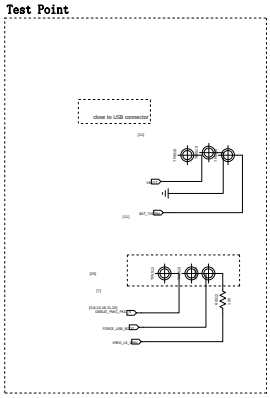
GPIO_0	TS_RST_N	GPIO_37	UIM1_CLK	GPIO_74	NC		
GPIO_1	TS_INT_N	GPIO_38	UIM1_RESET	GPIO_75	NC		
GPIO_2	TS_I2C_SDA	GPIO_39	NC	GPIO_76	LCD_ID		
GPIO_3	TS_I2C_SCL	GPIO_40	UIM_BATT_ALARM	GPIO_77	NC		
GPIO_4	MSM_UART_TX	GPIO_41	DSI_RST_N	GPIO_78	NC		
GPIO_5	MSM_UART_RX	GPIO_42	NC	GPIO_79	NC		
GPIO_6	NC	GPIO_43	PA_ON0	GPIO_80	ALSP_INT_N		
GPIO_7	NC	GPIO_44	PA_ON1	GPIO_81	ACCL_INT1		
GPIO_8	NC	GPIO_45	PA_ON2	GPIO_82	ACCL_INT2		
GPIO_9	NC	GPIO_46	PA_ON3	GPIO_83	NC		
GPIO_10	SENSORS_I2C_SDA	GPIO_47	NC	GPIO_84	NC		
GPIO_11	SENSORS_I2C_SCL	GPIO_48	NC	GPIO_85	WC_PWDN		
GPIO_12	DSI_LCD_TE0	GPIO_49	PA0_RANGE0	GPIO_86	NC		
GPIO_13	CAM_MCLK0	GPIO_50	PA0_RANGE1	GPIO_87	NC		
GPIO_14	CAM_MCLK1	GPIO_51	ANT_SW_SEL0	GPIO_88	NC		
GPIO_15	CAM2_RST_N	GPIO_52	ANT_SW_SEL1	GPIO_89	NC		
GPIO_16	CCI_I2C_SDA	GPIO_53	ANT_SW_SEL2	GPIO_90	BOOT_CONFIG_11		
GPIO_17	CCI_I2C_SCL	GPIO_54	NC	GPIO_91	NC		
GPIO_18	NC	GPIO_55	NC	GPIO_92	AUDIO_PA_EN		
GPIO_19	CAM_SMDVDD_EN	GPIO_56	NC	GPIO_93	NC		
GPIO_20	CAM1_STANDBY_N	GPIO_57	NC	GPIO_94	NC		
GPIO_21	CAM1_RST_N	GPIO_58	NC	GPIO_95	NC		
GPIO_22	BT_SSBI	GPIO_59	NC	GPIO_96	NC		
GPIO_23	WLAN_DATA2	GPIO_60	NC	GPIO_97	NC		
GPIO_24	WLAN_DATA1	GPIO_61	NC	GPIO_98	BOOT_CONFIG_13		
GPIO_25	WLAN_DATA0	GPIO_62	NC	GPIO_99	BOOT_CONFIG_14		
GPIO_26	WLAN_SET	GPIO_63	GPS_EXT_CTL	GPIO_100	FORCE_USB_BOOT		
GPIO_27	WLAN_CLK	GPIO_64	CHO_SSBI_RX	GPIO_101	NC		
GPIO_28	FM_SSBI	GPIO_65	CHO_SSBI_TX_GPS				
GPIO_29	FM_DATA	GPIO_66	NC				
GPIO_30	BT_CTL	GPIO_67	NC				
GPIO_31	BT_DATA	GPIO_68	CHO_GSM_TX_PHASE_D0				
GPIO_32	UIM2_DATA	GPIO_69	CHO_GSM_TX_PHASE_D1				
GPIO_33	UIM2_CLK	GPIO_70	NC				
GPIO_34	UIM2_RESET	GPIO_71	NC				
GPIO_35	NC	GPIO_72	KPSNS0				
GPIO_36	UIM1_DATA	GPIO_73	KPSNS1				

TITLE:	88100_1_12(2100)	REV:	0V1
DOCUMENT NO.:	04_GPIO_MAP	SIZED:	A3
DEPARTMENT:	Hardware DEPT.		
COMPANY:	WINOTECH		
DESIGNER:	Last Saved Date: 2010/5/6	SHEET	4 OF 27



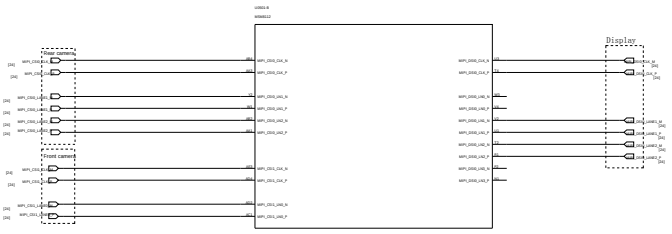
Mark Point

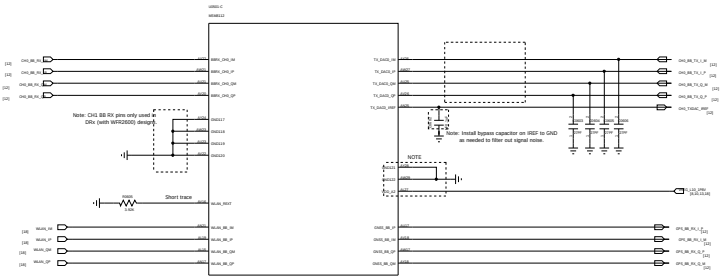
Test Point



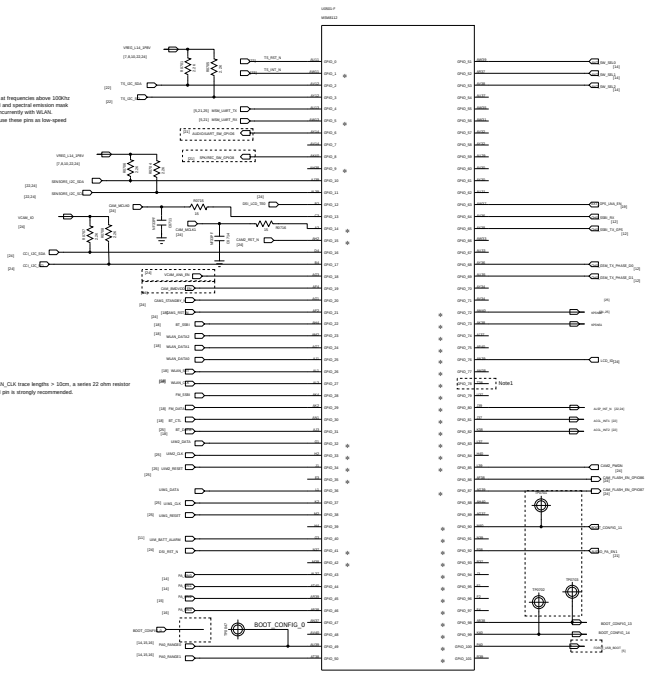
Shielding Frame

TITLE:	88100_1_12(Z100)	REV:	0V1
DOCUMENT NO.:	QS_MSM8X10_CONTROL_1	SIZE:	A3
DEPARTMENT:	Hardware DEPT.		
COMPANY:	WINOTECH		
DESIGNER:	Lee Sacred Dam 2015/5/8	SHEET:	5 OF 27





TITLE:	88100_1_12(Z1500)	REV:	0V1
DOCUMENT NO.:	QE_MSM8X10_CONTROL_2	SIZE:	A1
DEPARTMENT:	Hardware DEPT.		
COMPANY:	WINOTECH		
DESIGNER:	Last Saved Date: 2015/5/6	SHEET	6 OF 27



Note: Asterisks (*) indicate an MPM wake-able GPIOs. Refer to the device specification document (80-ND727-1) form more details.

Note: Do not have pull-ups on the following GPIOs unless intended for boot or secure-boot related configurations: GPIO 61, 62, 85, 90, 92, 98, 99, 100

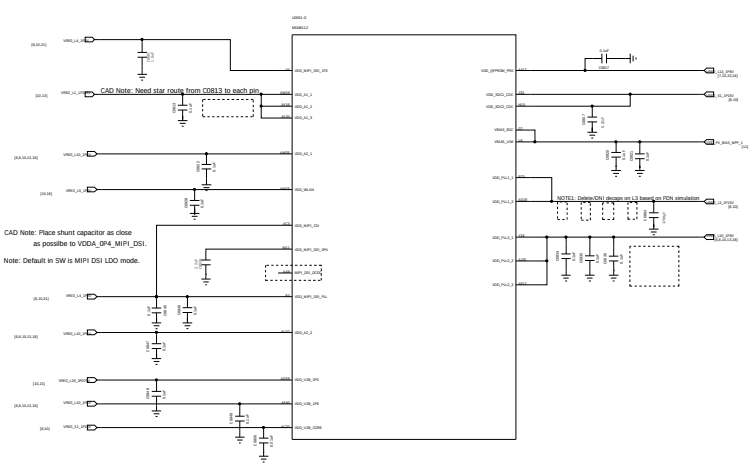
Note 1: If NFC is implemented, it is recommended to use GPIO_78 (GP_CLK_1A) as NFC clock. Sourcing the NFC clock from BBCLK1 is not recommended as clock degradation may occur.

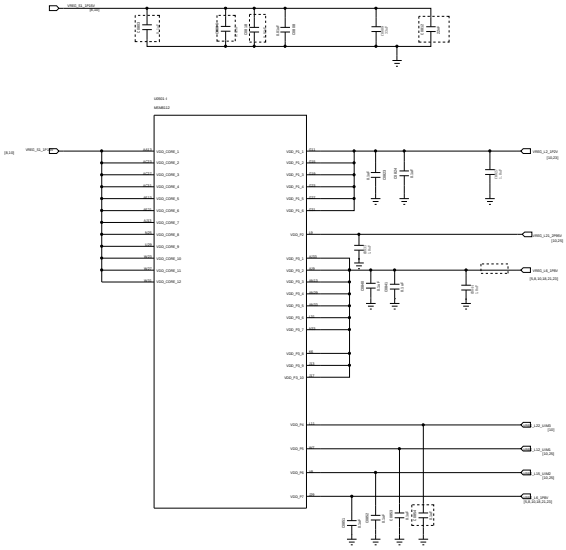
Backup for debug

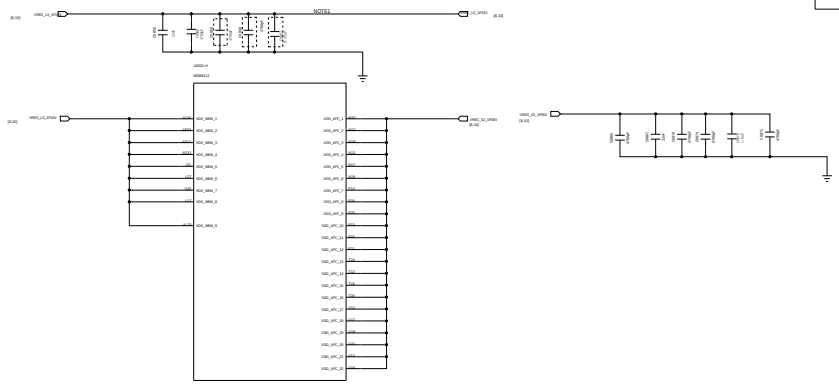
Configuration GPIO Table	
GPIO_49/ GMFC6	WDG_DISABLE
GPIO_50/ GMFC7	BOOT_CONFIG_1
GPIO_51/ GMFC8	BOOT_CONFIG_2
GPIO_52/ GMFC9	BOOT_CONFIG_3
GPIO_53/ GMFC10	BOOT_CONFIG_4
GPIO_55/ GMFC12	BOOT_CONFIG_5
GPIO_56/ GMFC13	BOOT_CONFIG_6
GPIO_57/ GMFC14	BOOT_CONFIG_7
GPIO_58/ GMFC15	BOOT_CONFIG_8
GPIO_59/ GMFC16	BOOT_CONFIG_9
GPIO_62/ GMFC19	BOOT_CONFIG_10
GPIO_80	BOOT_CONFIG_11
GPIO_82	BOOT_CONFIG_12
GPIO_83	BOOT_CONFIG_13
GPIO_85	BOOT_CONFIG_14
GPIO_85	BOOT_CONFIG_15
GPIO_100	FORCE_USB_BOOT

BOOT_OPTION_TYPE	FAST BOOT VALUE BOOT_CONFIG[4:1]	DESCRIPTION
BOOT_DEFAULT_OPTION	0b0000	eMMCSDC1 -> SDHSDC2 -> HSUSB2.0
BOOT_SDC_PORT2_THEN SDC_PORT1_OPTION	0b0001	SDHSDC2 -> eMMCHSDC1
BOOT_SDC_PORT1_OPTION	0b0010	eMMCHSDC1
BOOT_USB_OPTION	0b0011	HSUSB2.0
BOOT CONFIG GPIOs:BOOT_CONFIG[1] & BOOT_CONFIG[2]&BOOT_CONFIG[3]		
BOOT_CONFIG[0]: WDOG_DISABLE		

TITLE	80100_1_1321500	Rev.	EVT
DOCUMENT NO.	07_MSM8X10_GPIO	SIZE	A3
DEPARTMENT	Hardware DEPT.		
COMPANY	WINGTECH		
DESIGNER	Last Saved Date: 2015/11/6	SHEET	7 OF 27

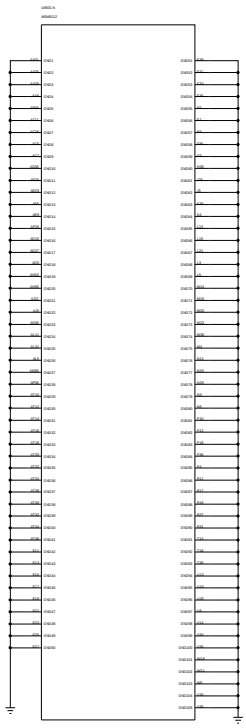






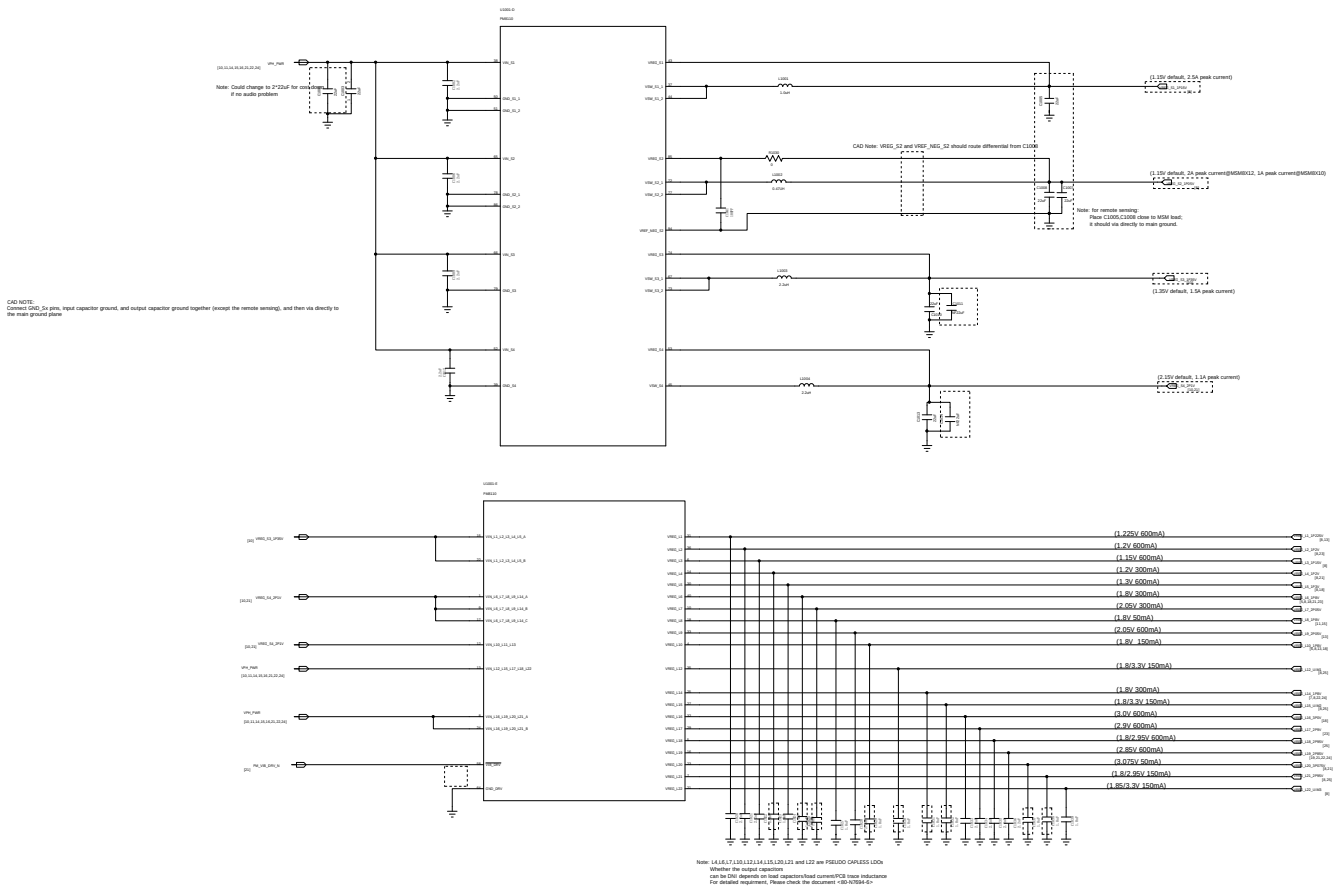
Note: Decoupling capacitor values and quantities are heavily dependent on layout. Customers must optimize decap configurations per power rail using PDN impedance specifications defined in 80-ND717-1 (Device Specification Document).

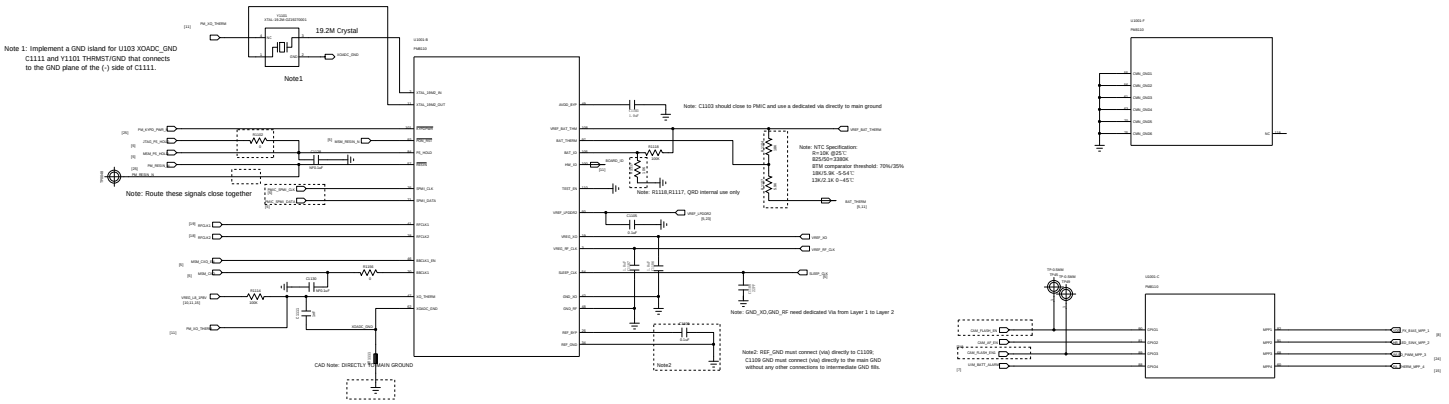
TITLE:	B810I_1_13(2100)	REV:	DVT
DOCUMENT NO:	08_MSM8X10_POWER_1	SIZE:	A3
DEPARTMENT:	Hardware DEPT.		
COMPANY:	INVENTEC		
DRAWN BY:	Last Saved Date: 2015/5/18	SHEET:	8 OF 27

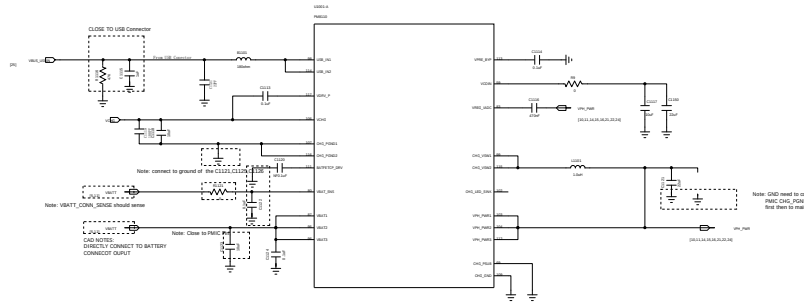


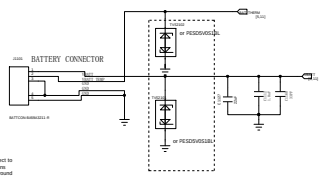


TITLE:	88100_1_12(2100)	REV:	0V/T
DOCUMENT NO.:	, 09_MSM8X10_GND	SIZE:	A1
DEPARTMENT:	Hardware DEPT.		
COMPANY:	WINOTECH		
DESIGNER:	Last Saved Date: 2015/1/9	SHEET:	9 OF 27

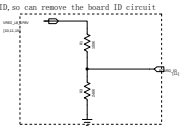

U1600-D
PM8150
VPH_PWR
[10,11,14,15,16,21,22,24]
Note: Could change to 2*22uF for consumer if no audio problem
VIN_S1
VIN_S2
VIN_S3
VIN_S4
VSW_S1_1
VSW_S1_2
VSW_S2_1
VSW_S2_2
VSW_S3
VSW_S4
GND_S1_1
GND_S1_2
GND_S2_1
GND_S2_2
GND_S3
GND_S4
VREG_S1
VREG_S2
VREF_SEC_S2
VREG_S3
VREG_S4
L1601
0.54uH
L1602
0.47uH
L1603
2.2uH
L1604
2.2uH
R1600
0
(1.15V default, 2.5A peak current)
(1.15V default, 2A peak current@MSM8X12, 1A peak current@MSM8X10)
(1.25V default, 1.5A peak current)
(2.15V default, 1.1A peak current)
CAD Note: VREG_S2 and VREF_NEG_S2 should route differential from C1006
Note: for remote sensing:
Place C1005,C1006 close to MSM load;
it should via directly to main ground.
CAD NOTE:
Connect GND_S4 pins, input capacitor ground, and output capacitor ground together (except the remote sensing), and then via directly to the main ground plane
U1600-E
PM8110
VREG_S1_VPRH
VREG_S4_1P25V
VREG_S4_2P5V
VPH_PWR
[10,11,14,15,16,21,22,24]
PM_VIB_DRV_N
VIN_L1_L2_L3_L4_L5_A
VIN_L1_L2_L3_L4_L5_B
VIN_L6_L7_L8_L9_L14_A
VIN_L6_L7_L8_L9_L14_B
VIN_L6_L7_L8_L9_L14_C
VIN_L10_L11_L13
VIN_L12_L15_L17_L18_L22
VIN_L16_L19_L20_L23_A
VIN_L16_L19_L20_L23_B
GND_DRV
VREG_L1
VREG_L2
VREG_L3
VREG_L4
VREG_L5
VREG_L6
VREG_L7
VREG_L8
VREG_L9
VREG_L10
VREG_L11
VREG_L12
VREG_L13
VREG_L14
VREG_L15
VREG_L16
VREG_L17
VREG_L18
VREG_L19
VREG_L20
VREG_L21
VREG_L22
VREG_L23
(1.225V 600mA)
(1.2V 600mA)
(1.15V 600mA)
(1.2V 300mA)
(1.3V 600mA)
(1.8V 300mA)
(2.05V 300mA)
(1.8V 50mA)
(2.05V 600mA)
(1.8V 150mA)
(1.8/3.3V 150mA)
(1.8V 300mA)
(1.8/3.3V 150mA)
(3.0V 600mA)
(2.9V 600mA)
(1.8/2.95V 600mA)
(2.85V 600mA)
(3.075V 50mA)
(1.8/2.95V 150mA)
(1.85/3.3V 150mA)
Note: L4,L6,L7,L10,L12,L14,L15,L20,L21 and L22 are PSEUDO CAPLESS LDOs
Whether the output capacitors
can be DNI depends on load capacitors/load current/PCB trace inductance
For detailed requirment, Please check the document <80-N7694-6>
TITLE: 88100_1_12(2100)
REV: 0VT
DOCUMENT NO.: 10_PM8110_PWR
SIZE: A1
DEPARTMENT: Hardware DEPT.
COMPANY: WINGTECH
DESIGNER:
Last Saved Date: 2015/5/8
SHEET: 10 OF 27







LPDDR2 have ID, so can remove the board ID circuit

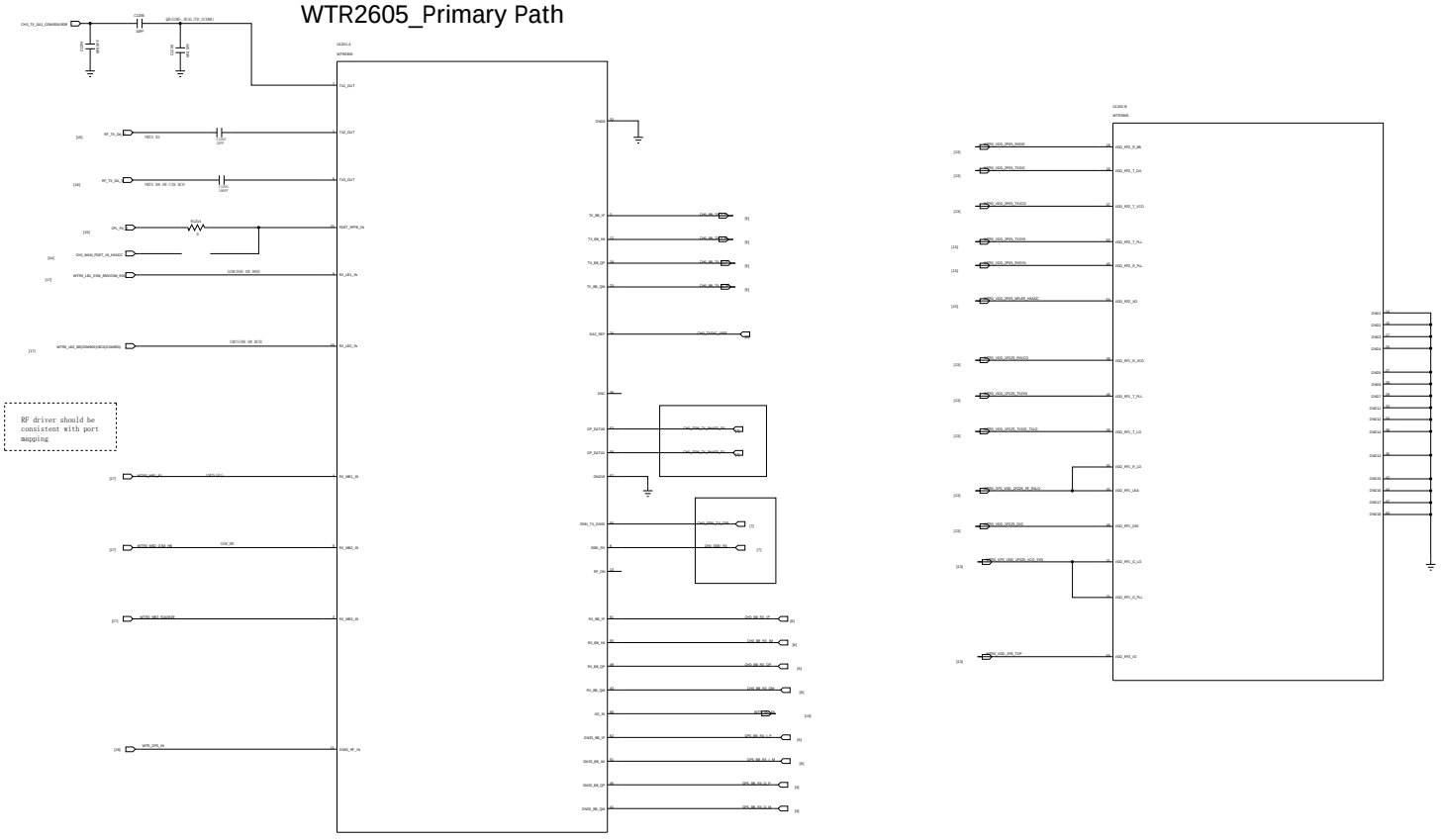


configure ID

R1	R3	Configure	
100K	240K	B1/BB/2sim-A1	1.27V
240K	100K	B2/BS/1sim	0.529V
100K	NF	B1/BB/1sim	1.8V
NF	240K	B2/BS/2sim-B1	0V

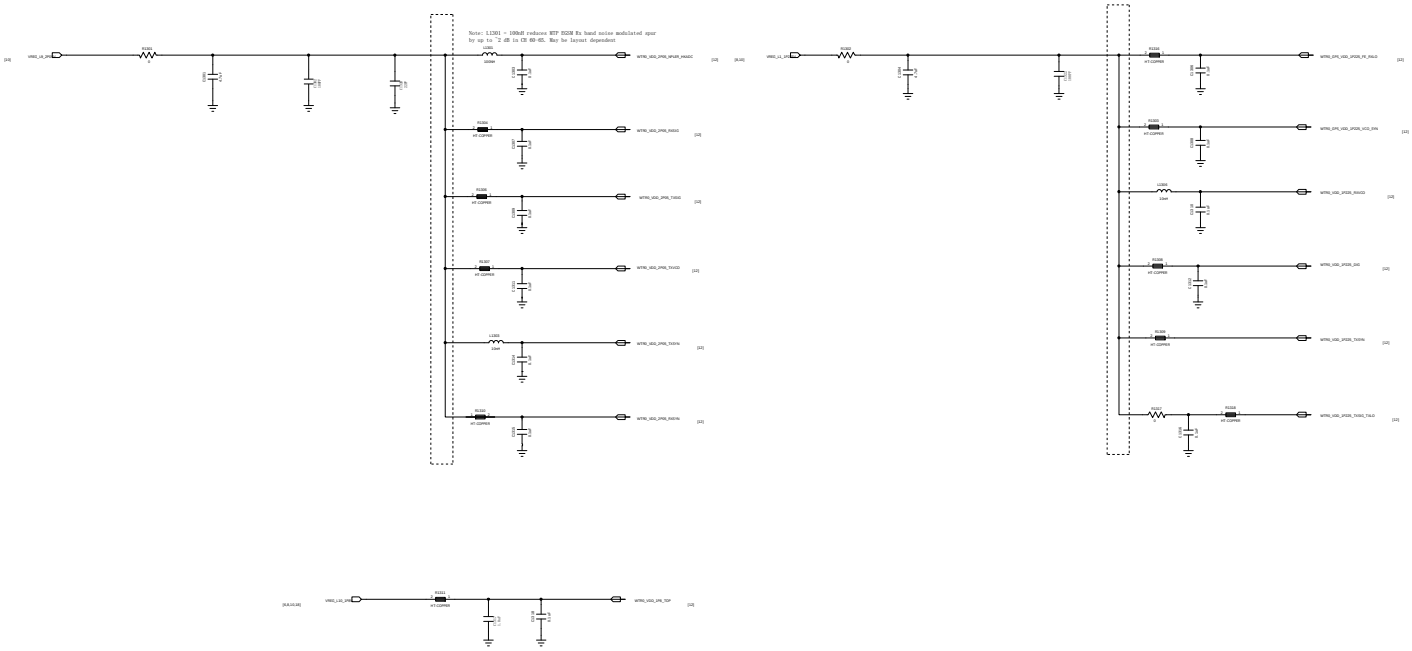
TITLE:	88100_1_12(2100)	REV:	0VT
DOCUMENT NO.:	,11_PM8110_CONTROL	SIZE:	A1
DEPARTMENT:	Hardware DEPT.		
COMPANY:	WINOTECH		
DESIGNER:	Last Saved Date: 2010/5/6	SHEET	11 OF 27

WTR2605_Primary Path

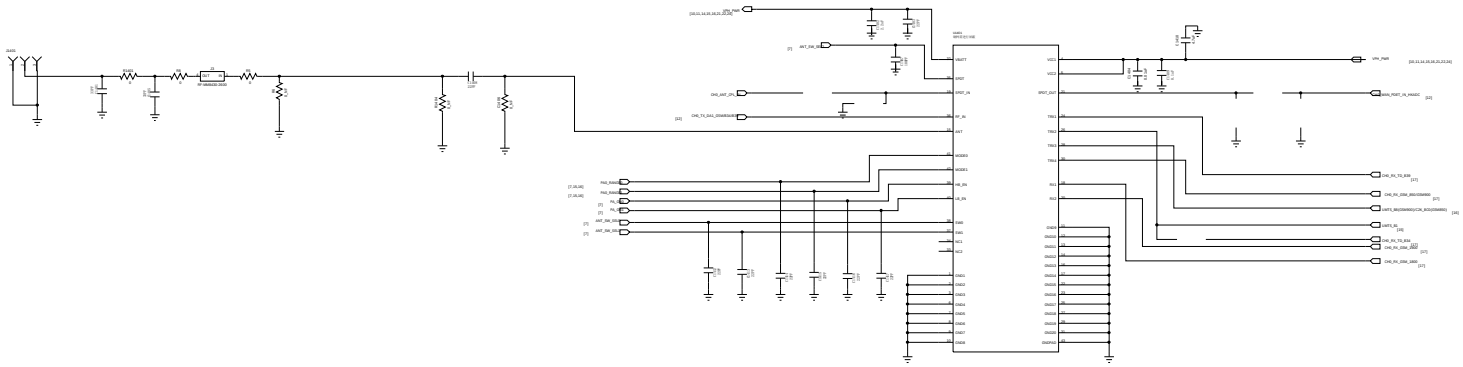


TITLE:	88100_1_12(2100)
DOCUMENT NO.:	12_WTR2605_PRIMARY_PATH
DEPARTMENT:	Hardware DEPT.
COMPANY:	WINOTECH
DESIGNER:	Date Saved Date: 2019/5/9
REV:	OVT
SIZE:	A3
SHEET	12 OF 27

WTR2605_Primary path_ Power Distribution 2.05V,1.8V,1.225V



TITLE:	88100_1_12(2100)	REV:	0V1
DOCUMENT NO.:	13_WTR2605_POWER_PRIMARY_PATH	SIZE:	A1
DEPARTMENT:	Hardware DEPT.		
COMPANY:	WINOTECH		
DESIGNER:	Last Saved Date: 2010/5/6	SHEET	13 OF 27

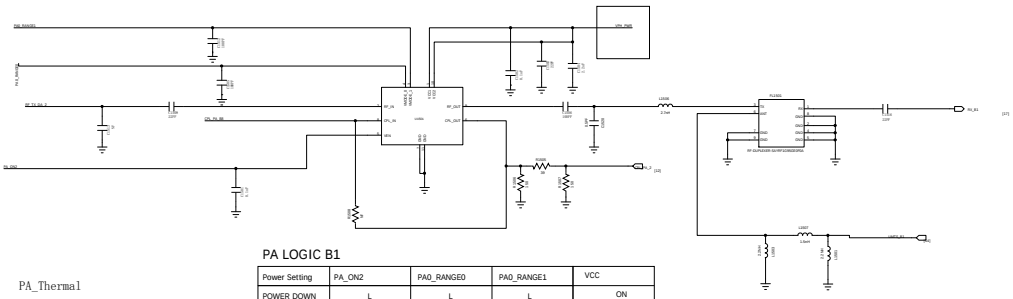


CH0 TxM PA/Switch Logic Table

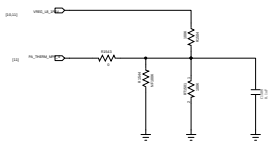
	CH0_					PA_RANGE			
	SPDT	SW1	SW0	HB_EN	LB_EN	Mode0	Mode1		
GSM850_TX_LB_SPDT_Off	0	0	1		0	0		X	X
GSM850_RX_TRX3_SPDT_0	1	0	1		0	1		X	X
GSM900_TX_LB_SPDT_Off	0	0	1		0	0		X	X
GSM900_RX_TRX2_SPDT_0	1	0	0		1	1		X	X
DCS1800_TX_HB_SPDT_Off	0	1	0		0	0		X	X
DCS1800_RX_RX2	1	1	1		1	1		X	X
PCS1900_TX_HB_SPDT_Off	0	1	0		0	0		X	X
PCS1900_RX_RX1	1	1	1		1	0		X	X
B1_TRX4_SPDT_0	1	0	1		1	1		X	X
B8_TRX3_SPDT_0	1	0	1		0	1		X	X
B34_TX_SPDT_0	0	1	0		1	0		X	X
B34_RX_TRX4_SPDT_0	1	0	1		1	1		X	X
B39_TX_SPDT_0	0	1	0		1	0		X	X
B39_RX_TRX1_SPDT_0	1	0	0		0	1		X	X
BC0_TRX3_SPDT_0	1	0	1		0	1		X	X

TITLE:	88100_1_12(21500)	REV:	0V1
DOCUMENT NO.:	14_WZR2605_TXM_PRIMARY_PATH	SIZE:	A1
DEPARTMENT:	Hardware DEPT.		
COMPANY:	WINOTECH		
DESIGNER:	Date: Second Date: 2015/5/9	SHEET:	14 OF 27

B1



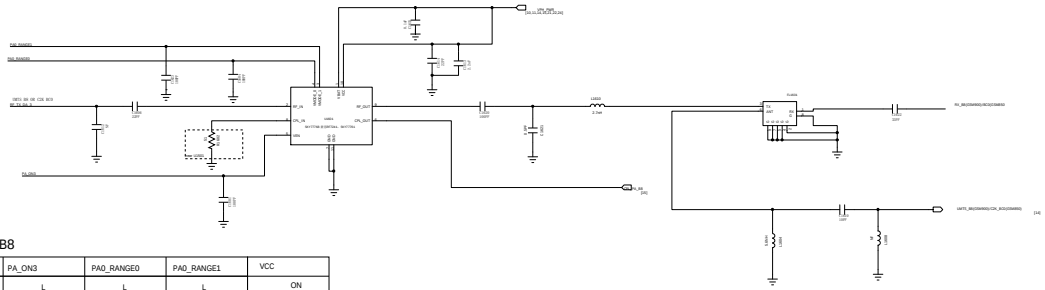
PA_Thermal



PA LOGIC B1

Power Setting	PA_ON2	PA0_RANGE0	PA0_RANGE1	VCC
POWER DOWN	L	L	L	ON
Standby Mode	L	—	—	ON
High Power	H	L	—	ON
Medium Power	H	H	L	ON
Low Power	H	H	H	ON

TITLE:	88100_1_12(2100)	Rev.	ENT
DOCUMENT NO:	15_UMTS_B1_PRIMARY_PATH	SIZE:	A0
DEPARTMENT:	Hardware DEPT.		
COMPANY:	WINGTECH		
DESIGNER:	Last Saved Date: 2019/1/16	SHEET	15 OF 27

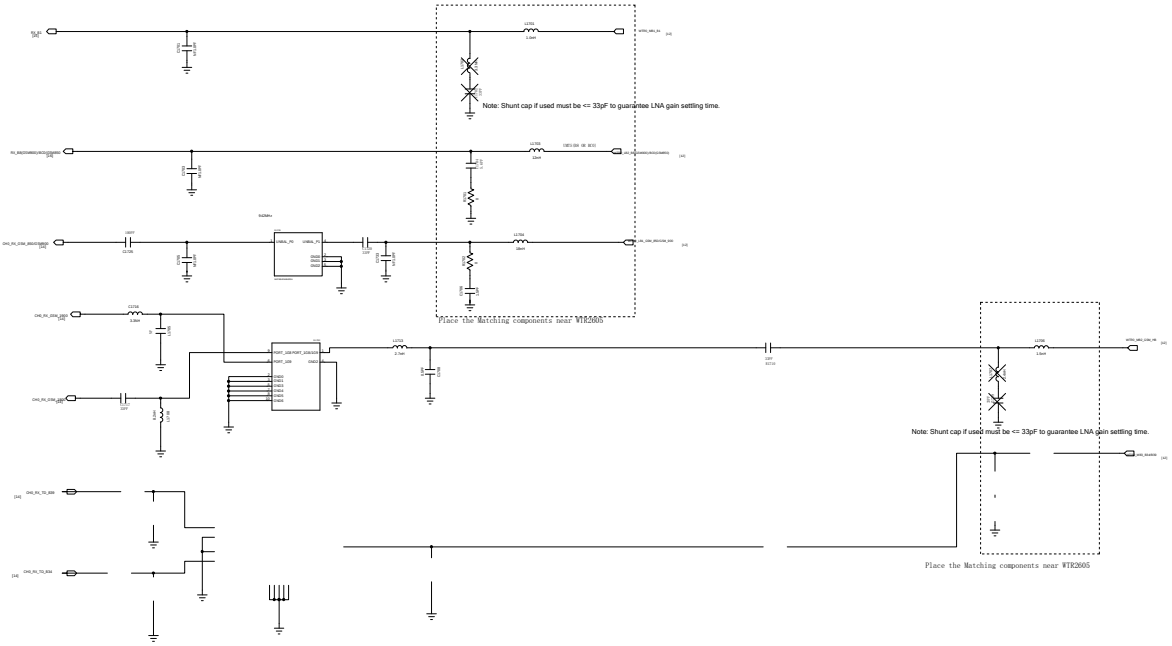


PA LOGIC B8

Power Setting	PA_ON3	PA0_RANGE0	PA0_RANGE1	VCC
POWER DOWN	L	L	L	ON
Standby Mode	L	——	——	ON
High Power	H	L	——	ON
Medium Power	H	H	L	ON
Low Power	H	H	H	ON

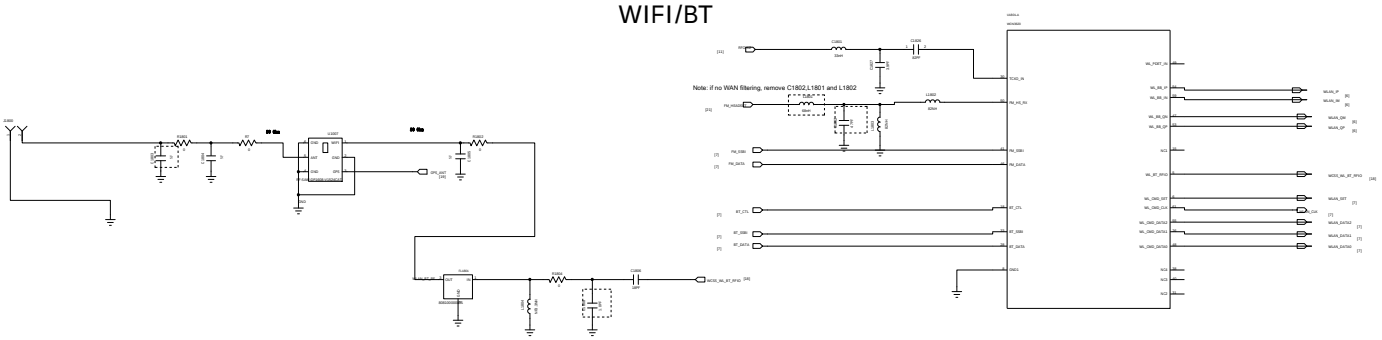
TITLE:	88100_1_12(2100)	REV:	OVT
DOCUMENT NO.:	16_UMTS_B8_PRIMARY_PATH	SIZE:	A1
DEPARTMENT:	Hardware DEPT.		
COMPANY:	WINOTECH		
DESIGNER:	Last Saved Date: 2015/3/9	SHEET	16 OF 27

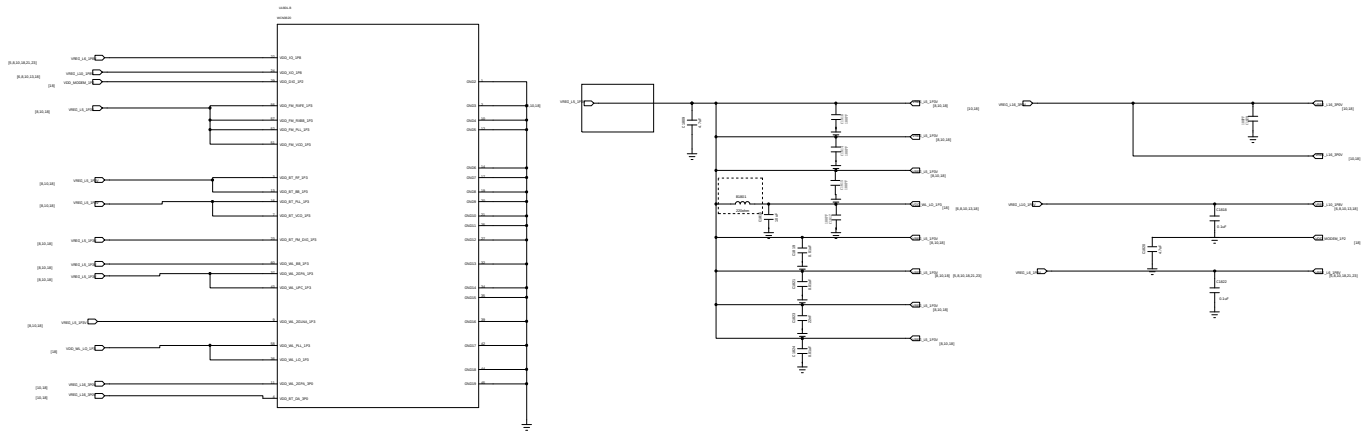
Primary PRX matching



TITLE:	88100_1_12(2100)	REV:	0V/T
DOCUMENT NO.:	17_PRX_MATCHING_PRIMARY_PATH	SIZE:	A1
DEPARTMENT:	Hardware DEPT.		
COMPANY:	WINNOTECH		
DESIGNER:	Last Saved Date: 2015/1/9	SHEET:	17 OF 27

WIFI/BT

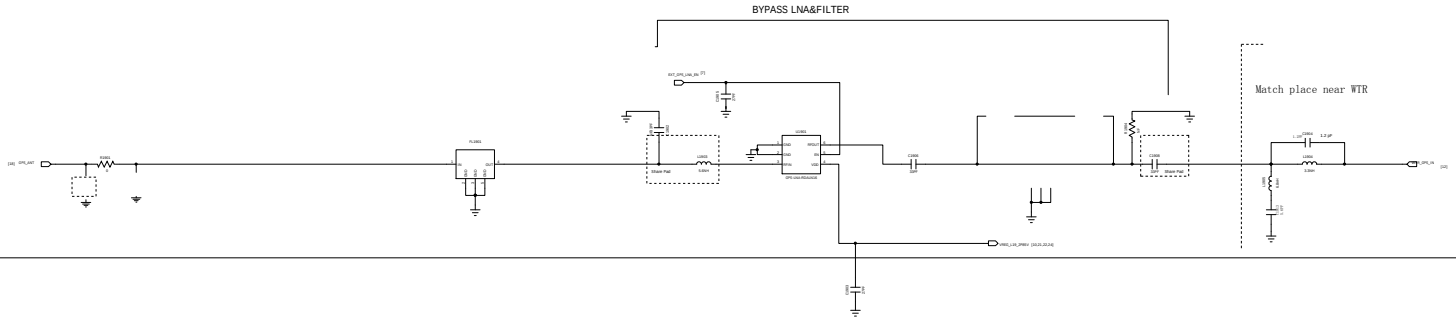




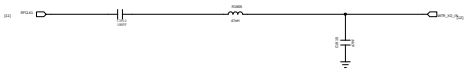
TITLE:	88100_1_12(2300)
DOCUMENT NO.:	18_WIFI/BT
DEPARTMENT:	Hardware DEPT.
COMPANY:	WINOTECH
DESIGNER:	Last Saved Date: 2015/5/19

REV: OVT
SIZED: A3
SHEET 18 OF 27

GPS

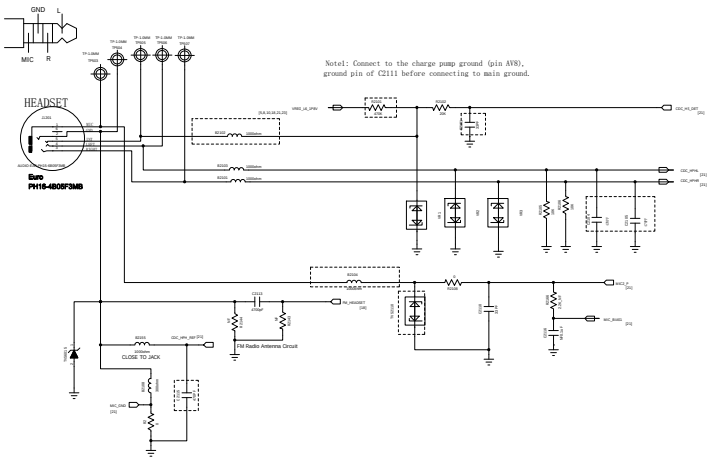


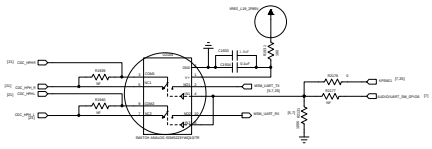
XO DISTRIBUTION

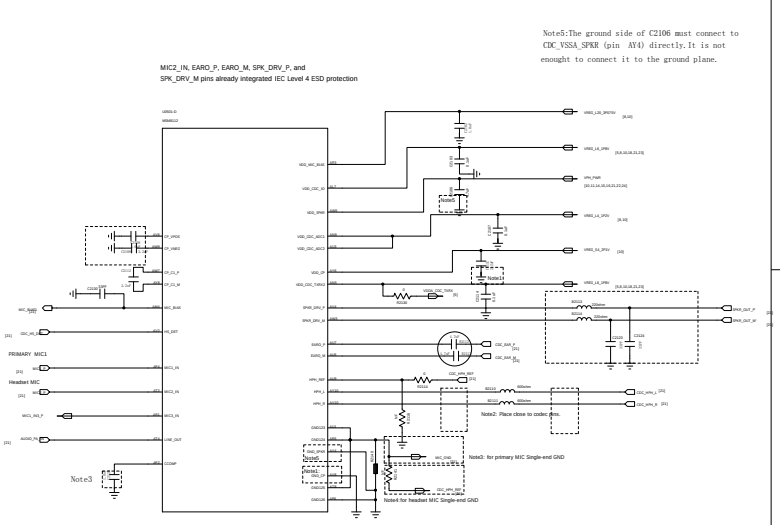


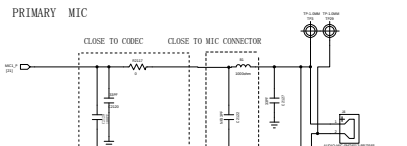
TITLE:	88100_1_12(2100)	REV:	0V1
DOCUMENT NO.:	19_GPS/XO_DISTRIBUTION	SIZE:	A1
DEPARTMENT:	Hardware DEPT.		
COMPANY:	WINOTECH		
DESIGNER:	Last Saved Date: 2015/5/9	SHEET:	19 OF 27

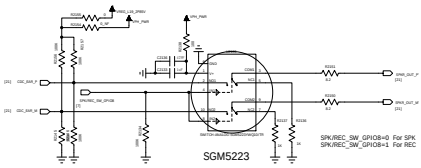
customer can refer QRD8x10 schematic for NFC HW design.

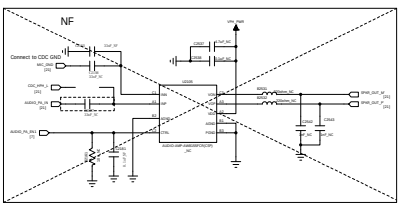


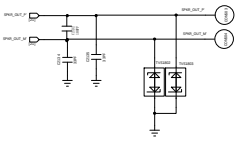


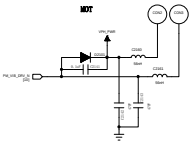








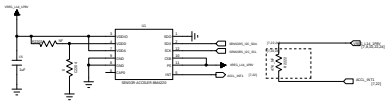




TITLE:	88100_1_12(2100)	REV:	0V1
DOCUMENT NO.:	21_AUDIO/MOT	SIZE:	A1
DEPARTMENT:	Hardware DEPT.		
COMPANY:	SUNNOTECH		
DESIGNER:	Date Saved Date: 2010/5/9	SHEET	21 OF 27

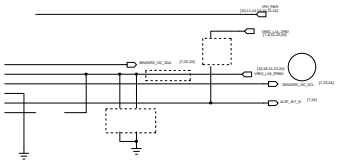
Accelerometer Sensor

compatible with KXCJK/LIS3DE

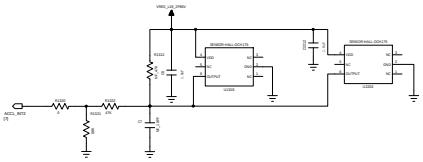


KXTJ2-1009

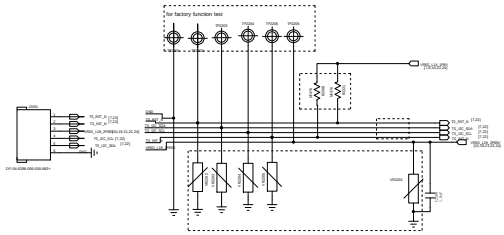
Ambient Light & Proximity Sensor



HALL

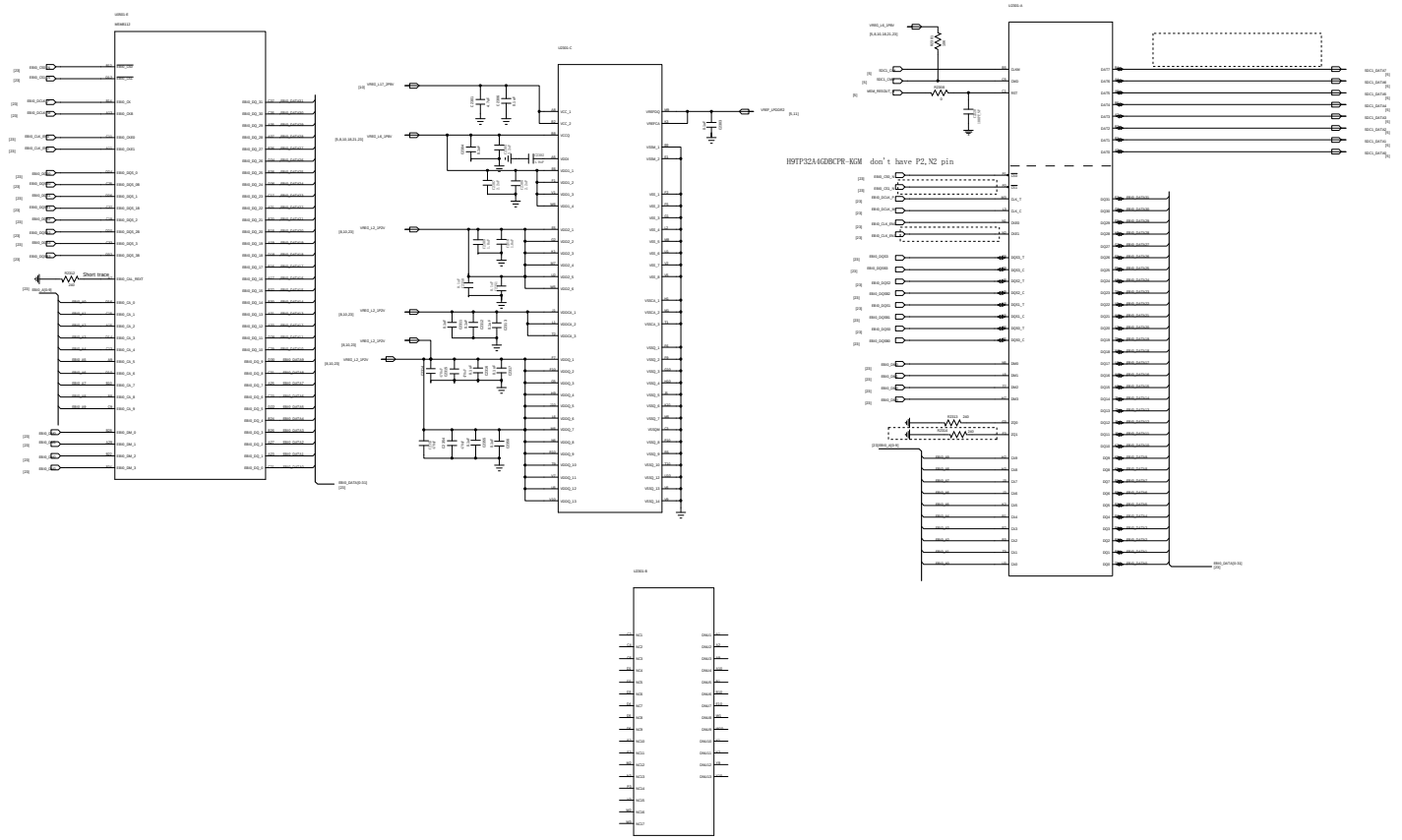


Capacitor Touch Panel



I2C Address	
Write	
Read	

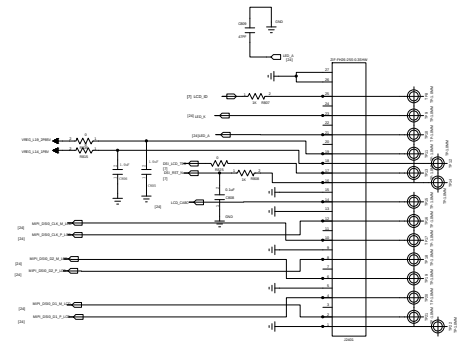
TITLE:	88100_1_12(2100)	REV:	DVT
DOCUMENT NO.:	22_SENSORS	SIZE:	A3
DEPARTMENT:	Hardware DEPT.		
COMPANY:	BIJINGTECH		
DESIGNER:	Last Saved Date: 2018/3/16	SHEET	22 OF 27



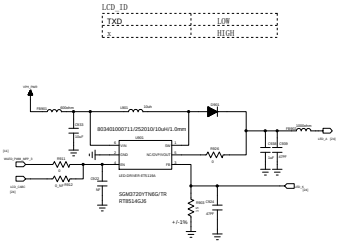
Note: Follow the memory vendor recommendations on decoupling capacitor configuration.

TITLE:	88100_1_12(2300)	REV:	0V1
DOCUMENT NO.:	23_MEMORY	SIZE:	A3
DEPARTMENT:	Hardware DEPT.		
COMPANY:	WINOTECH		
DESIGNER:	Date: Second Date: 2019/5/9	SHEET	23 OF 27

Main LCM

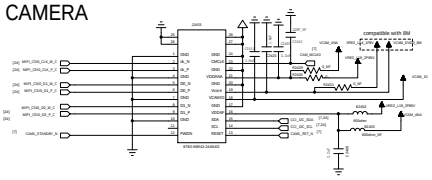


LCM: ILI9806E (TXD) CTP: MSG2233
HX8379C(YAXing)



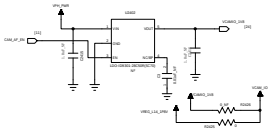
Backlight LED Driver

MAIN CAMERA

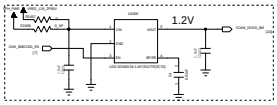


5M OV5670

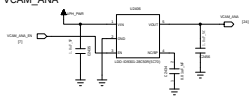
CAMIO LDO



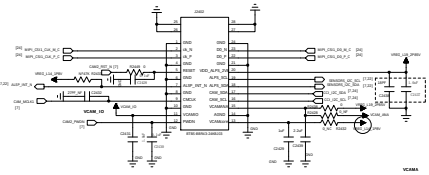
DVDD LDO



VCAM_ANA

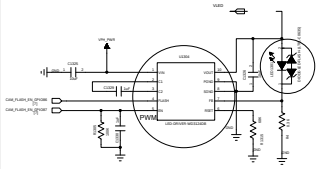


SUB CAMERA+ALPS sensor



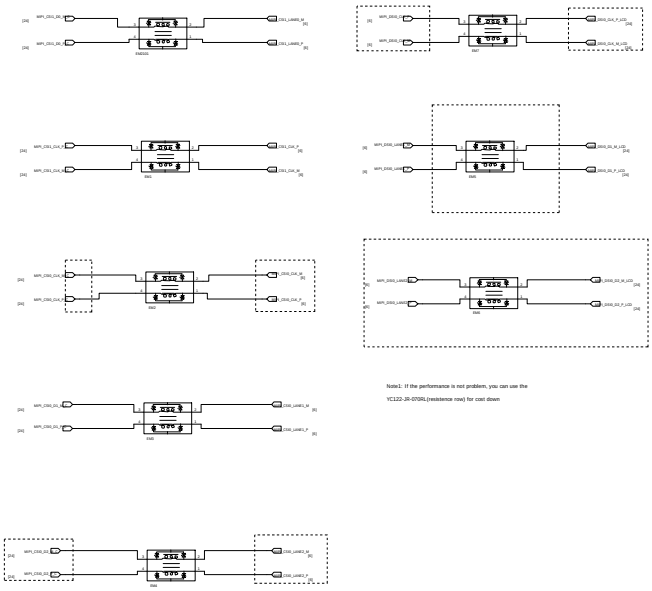
0.3M GC0310M
SP0A20
ALPS sensor LTR-553ALS-WA 0x23H-7bit/0x46H-write/0x47H-read

FLASH LED



Torch=0.05/Rfb
Flash=14.3K/Rset/Rfb

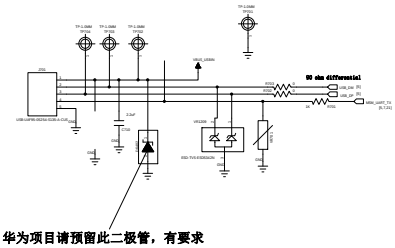
Rfb=0.22 Rset=82k I=800mA
Rfb=0.22 Rset=68k I=950mA



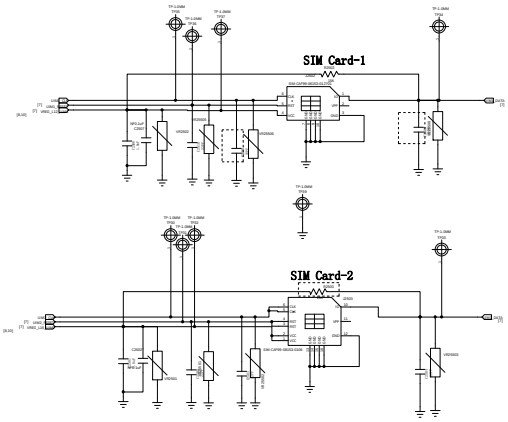
Note1: If the performance is not problem, you can use the YC122-JR-0709L(resistence row) for cost down

TITLE:	88100_1_12(2100)	REV:	0V7
DOCUMENT NO.:	24_MULTIMEDIA	SIZE:	A1
DEPARTMENT:	Hardware DEPT.		
COMPANY:	WINSTECH		
DESIGNER:	Last Saved Date: 2010/1/6	SHEET:	24 OF 27

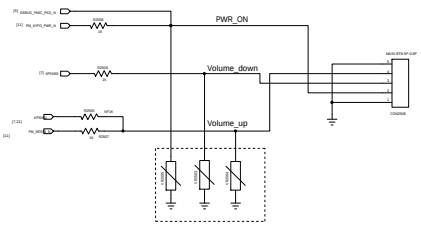
USB Connector



SIM Card

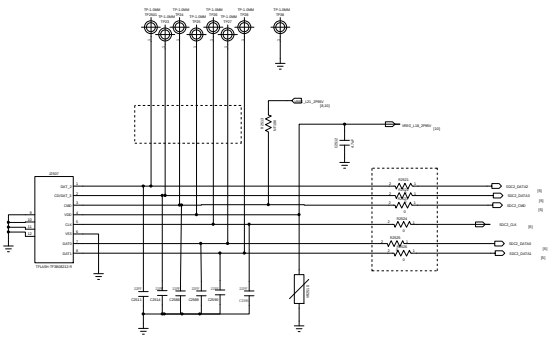


SIDEKEYS



Signal	Description
KPSNS0	Volume Down
PM_RESIN_N	Volume Up
KYPD_PWR_N	PWR_ON
PM_RESIN_N KYPD_PWR_N	Hardware Reset

MICRO SD



TITLE:	88100_1_12(2100)
DOCUMENT NO.:	25_INTERFACE
DEPARTMENT:	Hardware DEPT.
COMPANY:	WINGTECH
DESIGNER:	Date: Second Draft: 2010/5/6

REV: OVT
SIZED: A3
SHEET 25 OF 27

	Change List1

TITLE:	88100_1_12(2100)
REV:	0V7
DOCUMENT NO:	26_CHANGE_LIST1
SIZE:	A3
DEPARTMENT:	Hardware DEPT.
COMPANY:	JINGTECH
DESIGNER:	
Last Saved Date:	2016/5/6
SHEET:	26 OF 27

	Change List2

TITLE:	88100_1_12(2100)
REV:	0V/T
DOCUMENT NO.:	27_CHANGE_LIST2
SIZE:	A3
DEPARTMENT:	Hardware DEPT.
COMPANY:	WINSTECH
DESIGNER:	
Last Saved Date:	2015/1/9
SHEET:	27 OF 27